4.5 ANALOG CONTROL INTERFACE

The circuitry described in this section performs the following functions:

(1) Provides a two-way interface via a serial data link between out-guard digital processing and in-guard analog control circuitry on the reference divider pcb. (See Fig. 4.5.1).

(2) Monitors the CPU operation, serial transfer, digital supply failure and restart operations (watchdog), imposing a controlled safety default condition if there is a danger of losing digital control of the analog functions.

A manual reset of the safety monitor is provided on the front panel. (See Fig. 4.5.4).

4.5.1 General

Safety and Control information is input from Digital (400534) and Front (400533) Assemblies to out-guard circuits located on the Analog Interface Assembly (400570), processed and transferred across the 'Guard' isolation barrier to in-guard circuits in the Reference Divider Assembly (400535). After further processing in the Reference Divider Assembly, safety and control information is output to the following assemblies:

Sine Source Assembly (400446),
AC Assembly (400447),
PA Assembly (400450),
Output Control Assembly (400550),
Current Assembly (400555), and
High Voltage Assembly (400565).

Certain selected 'Status' signals, originating in the analog assemblies, are returned to the CPU during the data transfer. Thus, the data link forms a continuous loop, as shown in Fig. 4.5.1.

4.5.2 Serial Data Transfer (Fig. 4.5.1)

(Circuit Diagrams: 430534 Page 7.2-2, 430570 Page 7.3-3, 430535 Page 7.4-4 and Page 7.5-5)

A bi-directional serial data link passes information across the guard isolation screen; conveying CPU instructions to control the in-guard analog circuitry, and transferring critical status signals from the guarded circuits back to the CPU.

The link is managed by a synchronous serial data adapter (SSDA) which, having first been loaded with three bytes of control instructions by the microprocessor; transmits the resultant 24-bit word across guard one bit at a time, via its Tx DATA channel.

The 48 bits necessary to control the analog circuitry thus require two successive 24-bit transmissions.

Simultaneously with each 24-bit transmission, the SSDA receives a 24-bit word via its Rx DATA channel, enabling the CPU to obtain the status of the analog functions.

4.5.2.1 The Transfer Cycle (Fig. 4.5.1)

The CPU uses an address-code signal $\overline{\text{AN I/F STRT}}$ (Analog Interface Start) to initiate each 24-bit shift, by triggering a separate clock generator (M2, M3, M4) which produces a burst of 24 clocks per shift. Data is clocked in a serial string through a continuous loop comprising:

the 48-bit, serial in/parallel out, analog control shift register;

the 16-bit, parallel in/serial out, status shift register;

back to the SSDA receiver (Rx DATA).

The serial data string is correctly located after two 24-bit shifts, so then the SSDA generates a strobe pulse which:

(1) Transfers the data present in the serial data string of the six 8-bit analog-control shift registers (M27, M25, M31, M19, M30, M15) into their enabled parallel output registers and onto the analog control bus.

When the strobe ends, further transfer is disabled and the registers' output data is latched.

(2) Injects the status data at each of the parallel inputs of the two 8-bit status shift registers (M18, M22) into corresponding locations in the serial data string.

When the strobe ends, the parallel inputs to the status registers are disabled.

After the strobe pulse, the CPU initiates a further circulation of serial data (including the status data), in order to obtain the status data and return the analog control bits to the SSDA Rx DATA register for parity checking by the CPU.

This extra (confirmatory) circulation requires three more 24-bit shifts, so a complete data transfer consists of five shifts. If no error is detected, the SSDA provides a trigger-enable to allow updates to prevent activation (BARK) of the watchdog circuits.

If an error is detected on the first transfer, the CPU activates a second complete transfer, and then a third if an error is detected on the second. If the error persists after the third transfer, the trigger-enable is withheld, and the instrument will shut-down under the control of the watchdog safety monitor.

All interfacing between out-guard and in-guard circuits is achieved using electrically-isolating opto-couplers.

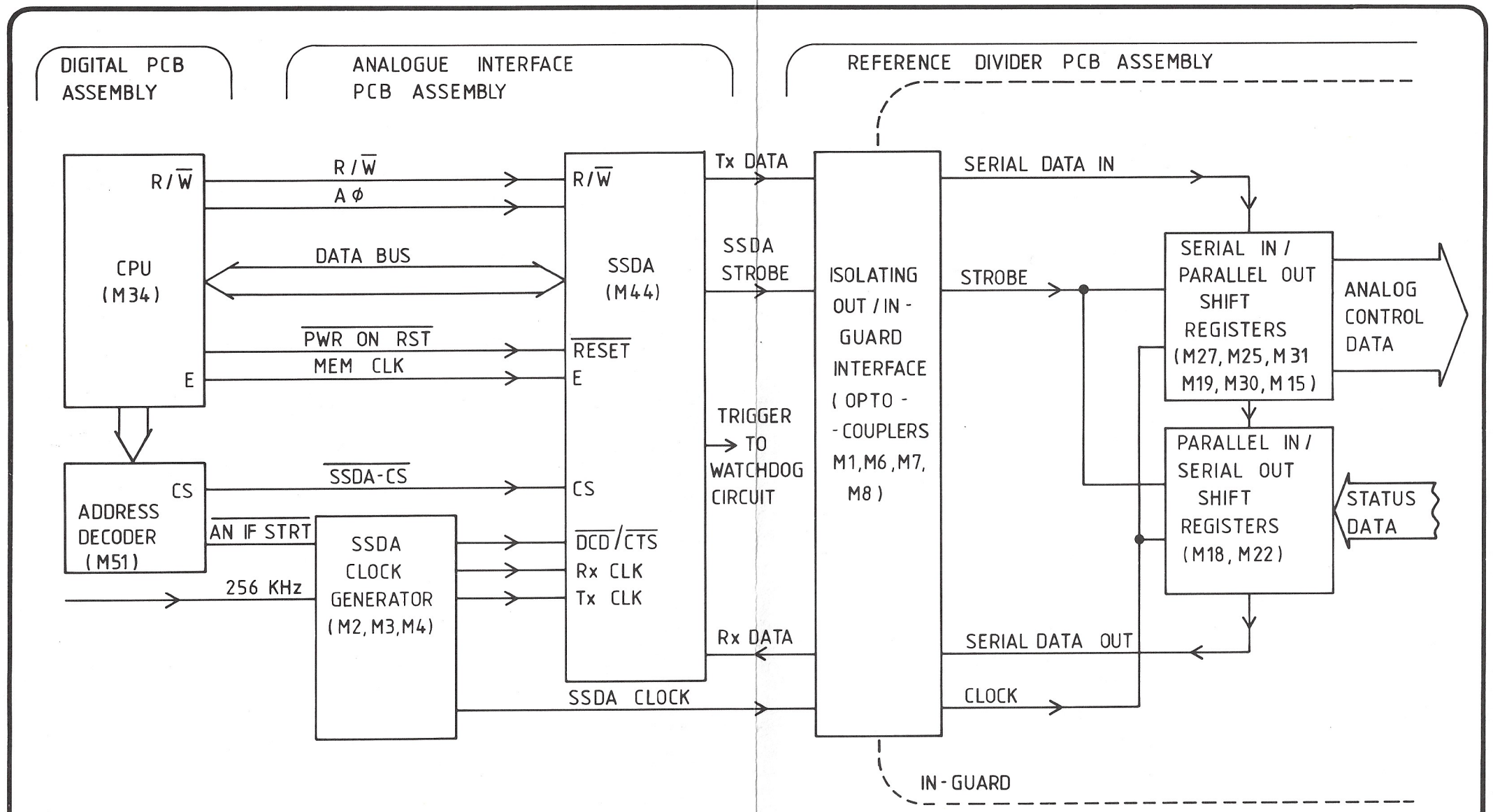


FIG. 4.5.1 SERIAL DATA LINK—SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

4.5.2.2 Data Transfer Organisation
(Fig. 4.5.2)

Data is transferred serially via the SSDA, control registers and status registers as directed by the CPU.

The exchange of data between the CPU and SSDA is made on the 8-bit instrument data bus, each exchange comprising three bytes (24 bits) of parallel data.

The shifts of serial data through the in-guard circuit are synchronized by clocks which are controlled from the CPU, and the SSDA Rx return registers are cleared when read by the CPU.

Once the in-guard serial data is correctly positioned at the inputs to the control registers, the SSDA generates a strobe which enables its transfer to the parallel outputs of the control registers. The same strobe enables injection of the data on the parallel inputs of the status registers into the serial data string.

The transfer operation requries five serial data shifts, each of three bytes, through the registers. During this operation: the control registers are loaded with bytes of new data (ND); the status registers are loaded with new status data (NS); and the whole of the ND and NS data is returned to the CPU, which:

a. verifies that the analog control bits of the serial data string return to the SSDA Rx DATA register without error. This confirmation indicates that at least, the correct bit pattern was applied to the analog control register inputs at the time the strobe was generated.

and

b. acts upon the status data received.

4.5.2.3 Transfer Sequence

The sequence of events in the transfer operation is as follows, refer to Fig. 4.5.2:

(A) Three bytes of new data, ND1, 2 and 3 are loaded into the SSDA transmitter registers; this data is destined for control registers D1, 2 and 3. The SSDA receiver registers were cleared when last read by the CPU.

(B) A burst of 24 clock pulses, initiated by the CPU, shifts all data three bytes to the right. After the shift is completed, the transmitter registers are loaded with new data bytes ND4, 5 and 6 (destined for control registers D4, 5 and 6). During this period, no transfers are made between the serial data string and the parallel control or status registers.

(C) A second burst of 24 clock pulses again shifts all data three bytes to the right. New data bytes ND1 to 6 are now correctly positioned in control registers D1-D6. After completion of the shift, three dummy bytes are loaded into the transmitter registers. Old data (OD) in the receiver register is ignored.

(D) With new data bytes ND1 to 6 correctly located, the SSDA generates a strobe pulse. This pulse:

(1) latches the 48 bits of bytes ND1 to 6 at the parallel outputs of control registers D1 to 6;

(2) enables the parallel inputs of status registers S1 and 2, loading two new status bytes NS1 and 2 and clearing old data OD5 and 6 from the registers.

(E) A third burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes NS1, NS2 and ND1 from the SSDA receiver registers (the CPU may take immediate action on NS returns). After the shift is complete, new data bytes ND1, 2 and 3 are re-loaded into the transmitter registers.

(F) A fourth burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes ND2, 3 and 4 from the receiver registers. After the shift is complete, new data bytes ND4, 5 and 6 are re-loaded into the transmitter registers.

(G) A fifth burst of 24 clocks again shifts all data three bytes to the right. Bytes ND5 and 6 are read from the receiver registers. The CPU has now read all new data and status bytes and the transfer sequence ends. If an error is detected between new data transmitted and new data received, the transfer process is repeated; three attempts are allowed before a fault condition is declared.

4.5.3 Synchronous Serial Data Adaptor
(Circuit Diagram 430570 Page 7.3-5)

4.5.3.1 SSDA Initialization

When power supplies are first switched on or an external reset EXT RST is applied, the signal $\overline{\text{PWR ON RST}}$ (Power On Reset) is held at logic-Ø for approximately 8ms.

During this period, the SSDA is latched in a reset condition to prevent erroneous output transitions at its Tx and Rx interfaces; the internal transmit registers are inhibited to prevent the loading of data from the data bus and the SSDA strobe output is held at logic-1.

After $\overline{\text{PWR ON RST}}$ returns to logic-1; the latches, registers and SSDA strobe are cleared in software, during the initialization routine.

4.5.3.2 Parallel Data Input From CPU

The conditions for parallel data on the data bus to be accepted by the SSDA are as follows:

(1) Chip-select $\overline{\text{SSDA CS}}$ at logic-Ø.

(2) Read/Write command R/$\overline{\text{W}}$ at logic-Ø. This controls the direction of data flow via the Data Bus through the SSDA input/output port. When R/$\overline{\text{W}}$ is at logic-Ø, data on the Data Bus is written into a selected register within the SSDA.

(3) The memory clock 'MEMCLK' 682.6kHz square wave is present to synchronize the SSDA operating cycle to that of the CPU.

With input conditions present as above and register address bit Ao at logic-1, the SSDA accepts data from the data bus into an internal 3-byte FIFO register. This data is entered over several MEMCLK cycles and stored in the FIFO register in readiness for serial transmission from the SSDA.

Software programming of the SSDA is performed when the address bit Ao is at logic-Ø. For details of 'Control Byte' operation, refer to Motorola 6852 data sheet.

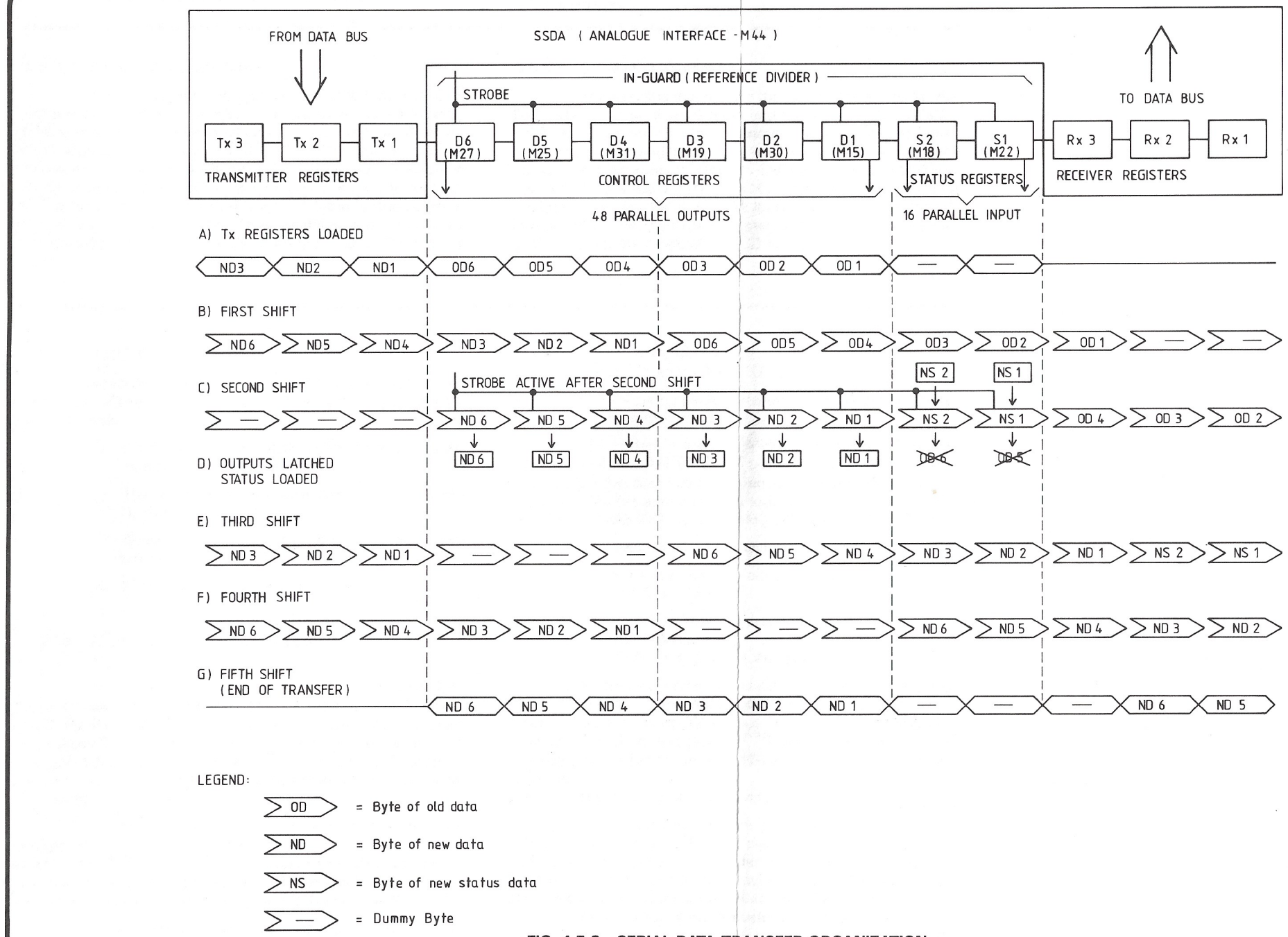


FIG. 4.5.2 SERIAL DATA TRANSFER ORGANIZATION

4.5.3.3 Parallel Data Output to CPU

The conditions for data to be read back from the SSDA on to the data bus are as follows:

(1) Chip-select $\overline{\text{SSDA CS}}$ at logic-Ø.

(2) Read/Write command R/$\overline{\text{W}}$ at Logic-1.

(3) Memory clock, MEM CLK, present.

The data read from the SSDA may be from one of two sources, selection being made by address bit Ao:

With Ao at logic-1, received data from the serial data input FIFO is transferred to the data bus.

With Ao at logic-Ø, the CPU reads an internal SSDA status register.

4.5.3.4 Serial Data Transmission

Serial data transmission is controlled by the $\overline{\text{CTS}}$ (clear to send) input to the SSDA. Transmission is inhibited by $\overline{\text{CTS}}$ at logic-1, and enabled when $\overline{\text{CTS}}$ is set to logic-Ø by the CPU address-code signal $\overline{\text{AN I/F STRT}}$. The first serial bit is transmitted by the negative transition of the first full positive Tx clock pulse (256 kHz) after $\overline{\text{CTS}}$ has been set to logic-Ø. $\overline{\text{CTS}}$ is held at logic-Ø by the $\overline{\text{AN I/F STRT}}$ latch for the duration of 24 full Tx clock pulses, thus enabling the serial shift transmission of the 24 data bits from the Tx Data FIFO in the SSDA.

4.5.3.5 Serial Data Reception

Serial data is received by the SSDA, controlled by the $\overline{\text{DCD}}$ (data carrier detect) level and clocked by Rx CLOCK. $\overline{\text{DCD}}$ is common to the transmit control $\overline{\text{CTS}}$ so that transmission to, and reception from the serial/parallel shift registers is synchronous. Both Rx CLOCK and Tx CLOCK have the same frequency but Rx CLOCK is inverted with respect to the latter. The first bit arriving at its Rx DATA input is clocked into the SSDA Receive FIFO register on the positive transition of the first full Rx clock after $\overline{\text{DCD}}$ is set to logic-Ø.

4.5.4 SSDA Clock Generation

Serial data is transmitted and received in bursts of 24 data bits. Three clocks are used to time the flow of bits, ensuring that:

(1) Data has time to settle before being clocked along the shift registers.

(2) The first Rx data sample is taken before it is lost by the first bit-shift.

(3) Subsequent Rx data has time to settle before being sampled by the SSDA.

(4) Exactly 24 bits are shifted in each burst.

4.5.4.1 SSDA, Tx and Rx Clock Action
(Fig. 4.5.3)

The three clocks are derived from the 256 kHz square wave output from the 13-bit counter (Circuit Diagram 430570 Page 7.3-2): The 256 kHz squarewave is used directly as 'Tx clock' into the SSDA. The negative transition of the first full positive pulse after $\overline{\text{CTS}}$ is set to logic-Ø; triggers the first serial Tx data bit setup (Refer to Fig. 4.5.3 Waveforms G and H).

'Rx clock' is an inverted version of the 256 kHz squarewave. The positive transition of the first full Rx clock cycle, after $\overline{\text{DCD}}$ is set to logic-Ø; triggers the SSDA to sample the first Rx data bit before the first SSDA clock has triggered the shift registers. (Refer to Fig. 4.5.3 Waveforms K and J).

'SSDA clock' is also an inverted version of the 256 kHz squarewave. The inversion allows approximately 2ms of data setup time for all serial data bits prior to clocking the data along the shift registers. SSDA clock is gated at M2-3 by the action of M3-12 to ensure that the first Rx data is sampled before it is lost by the first bit-shift. 24 SSDA clock pulses are counted by M4, allowing 24 bits to be shifted before resetting the Analog Interface Start latch M2-11 (TP3) to logic-1. (Refer to Fig. 4.5.3 Waveform I).

4.5.4.2 SSDA Clock Circuitry
(Circuit Diagram 430570 Page 7.3-3)

The following paragraphs describe the action of the SSDA clock generator circuitry.

The action of the SSDA clock generator is initiated by the command $\overline{\text{AN I/F STRT}}$ from the CPU. This occurs after the parallel data has been loaded into the SSDA transmit registers from the data bus. The logic-Ø pulse of $\overline{\text{AN I/F STRT}}$ sets flip-flop M2-10/11 to give a logic-Ø at TP3 which then:

(1) Sets the D input level of flip-flop M3-5;

(2) Removes 'set' to enable shift register M3 at M3-6 and M3-8;

(3) Removes 'reset' to enable counters M4 at M4-7 and M4-15.
(Refer to Fig. 4.5.3 Waveforms A and C).

At the next rising edge of the inverted 256 kHz (Rx clock) from M43-8 after $\overline{\text{AN I/F STRT}}$, the shift register M3 is clocked but only M3-1 'Q' output changes state to logic-Ø. This is applied to the SSDA $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs, thus releasing the inhibits on the SSDA transmit and receive registers.
(Refer to Fig. 4.5.3 Waveforms D and E).

At the next (second) rising edge of the clock to M3, M3-12 changes to logic-1. This allows NAND M2-3 to pass 256 kHz clock pulses via buffer M5-12 to the Reference Divider Assembly as the clock which shifts the serial data string along the analog-control and status registers.
(Refer to Fig. 4.5.3 Waveforms D, F and I).

The 256 kHz clock at NAND M2-3 is applied to the 4-bit up-counter clock input at M4-1, each rising edge causing the counter to increment by 1.

The divide-by-16 output M4-6 is applied to the enable input at M4-10; the falling edge of this output occurs at count-16 and increments the second counter to give, at M4-11, a logic-1 output. At count-24, M4-6 changes again to logic-1, and together with M4-11 output, gives a logic-Ø from NAND M2-4, causing the following actions:

(1) Flip-flop M2-12 is reset to give logic-1 at TP3.

(2) The logic-1 at TP3 sets shift register M3 to give:

a. logic-1 at M3-1, thus inhibiting $\overline{DCD}$ and $\overline{CTS}$;

b. logic-Ø at M3-12, disabling NAND M2-3 and thus stopping any further SSDA clocks.

(3) The logic-1 at TP3 resets the up-counters M4 causing:

a. the counter outputs to fall to logic-Ø, inhibiting further counting;

b. NAND M2-5 to rise to logic-1, re-setting flip-flop M2-12 to prepare for the next $\overline{AN\ I/F\ STRT}$ input.

(Refer to Fig. 4.5.3 Waveforms I, B, C, E and F).

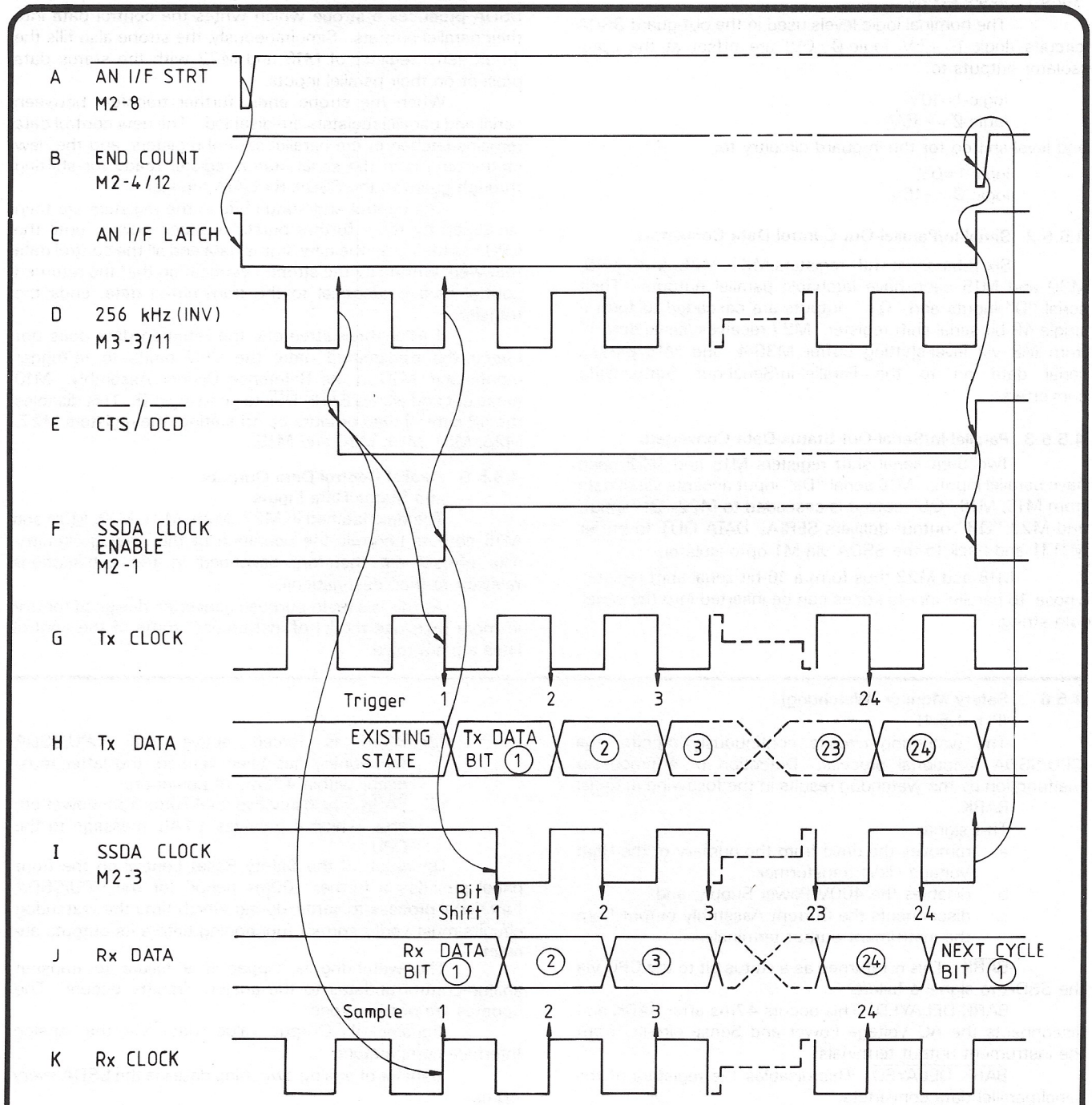


FIG. 4.5.3 SSDA CLOCK GENERATOR WAVEFORM

4.5.5 Serial/Parallel Data Converter

(Circuit Diagram 430535 Pages 7.4-4 and 7.4-5)

Serial control data transmitted from the SSDA (Analog Interface Assembly), together with their control signals (SSDA strobe and SSDA clock), enter the Reference Divider Assembly via the Mother Assembly.

The data and signals cross the isolation barrier through opto-isolators M6, M7 and M8 into guard.

Serial control and status data is returned out of guard to the SSDA receiver via opto-isolator M1.

4.5.5.1 Logic Levels

The nominal logic levels used in the out-guard SSDA circuits (logic-1=+5V, logic-Ø=0V) are offset at the opto-isolator outputs to:

logic-1=10V,
logic-Ø=-15V;

and level-shifted for the in-guard circuitry to:

logic-1=0V,
logic-Ø=-15V

4.5.5.2 Serial-In/Parallel-Out Control-Data Convertors

Six 8-bit serial shift registers M27, M25, M31, M19, M30 and M15 each have latchable parallel outputs. Their serial "D" inputs and "Q's" outputs are cascaded to form a single 48-bit serial shift register. M27 receives 'serial data in' from M8 via level-shifting buffer M36-4, and M15 passes serial data on to the Parallel-in/Serial-out Status-Data converters.

4.5.5.3 Parallel-In/Serial-Out Status-Data Converters

Two 8-bit serial shift registers M18 and M22 each have parallel inputs. M18 serial "Ds" input accepts serial data from M15; M18 "Q8" output is cascaded to M22 "Ds" input; and M22 "Q8" output delivers SERIAL DATA OUT to buffer M11-11 and back to the SSDA via M1 opto-isolator.

M18 and M22 thus form a 16-bit serial shift register whose 16 parallel inputs states can be inserted into the serial data string.

4.5.5.4 Serial Data Cycling

The serial data, organized in five blocks of three bytes (Refer to Section 4.5.2.2) is accompanied by synchronized bursts of 24 clocks. The output from opto-coupler M7 is buffered via level-shifter M36-2 and then inverted at M14-6. The timing of the positive clock edges allows all bits of serial data (distributed throughout the shift registers) to stabilize before being clocked on.

After the CPU has generated two bursts of data and clock pulses, the serial control data has shifted into the correct positions in control registers M27, M25, M31, M19, M30 and M15. So before the third burst of three bytes, the SSDA produces a strobe which writes the control data into their parallel outputs. Simultaneously, the strobe also fills the 16-bit serial register of M18 and M22 with the status data present on their parallel inputs.

When the strobe ends, further transfers between serial and parallel registers are disabled. The new control data remains latched in the parallel control registers, and the new status data is in the serial status register ready for shifting through guard to the SSDA Rx DATA register.

The control and status bits in the registers are then circulated by three further bursts of clock pulses, until the CPU has read both the new status data and all the control data that were written by the strobe. Verification that the returned control data is identical to the transmitted data, ends the transfer.

If after three attempts, the returned data does not match the transmitted data; the CPU omits to re-trigger monostable M10 in the Reference Divider Assembly. M10 times out and allows $\overline{\text{BARK DEL}}$ to go to logic-Ø. This disables the 48 control data outputs by 'tri-stating' the registers M27, M25, M31, M19, M30 and M15.

4.5.5.5 Parallel Control-Data Outputs and Status-Data Inputs

The data latched in M27, M25, M31, M19, M30 and M15 outputs controls the operation of the Analog circuitry. The effects are therefore described in the sub-sections relevant to their destinations.

As this is a multi-purpose converter, designed for use in more than one model of instrument, some of the control lines are not used.

4.5.6 Safety Monitor (Watchdog)

(Fig. 4.5.4)

The watchdog circuits continuously monitor the CPU/SSDA functional process. Detection of a processor malfunction by the watchdog results in the following actions:

BARK.

This signal:

a. removes the drive from the primary of the High Voltage (1kV) transformer,
b. disables the 400V Power Supply, and
c. disconnects the Current Assembly output from the instrument output terminals.

$\overline{\text{BARK}}$. This is returned as a status bit to the CPU via the SSDA to signal a failure.

BARK DELAYED. This occurs 47ms after BARK and disconnects the AC Voltage Power and Sense circuits from the instrument output terminals.

$\overline{\text{BARK DELAYED}}$. This disables the registers of the serial/parallel data converters.

The watchdog outputs are manipulated by the power-on are set circuits as follows:

(1) BARK DELAYED and $\overline{\text{BARK DELAYED}}$ are held active for 80ms from power-on and then are allowed to the inactive state only after two SSDA strobes have been detected.
(2) BARK is forced active until CPU/SSDA functioning has been verified; the latter must occur within 470ms of power-on.
(3) $\overline{\text{BARK}}$ is held inactive for 470ms from power-on, after which it provides a FAIL message to the CPU.

Operation of the Safety Reset control on the front panel provides a further 100ms period for the CPU/SSDA functional process to settle, during which time the watchdog circuits must verify correct functioning before its outputs are reset.

The watchdog is tripped if a failure to transmit analog-control updates to the analog circuitry occurs. The updates are of two types:

Transfer of 'Output value' data via the Analog Interface comparators,

Transfer of analog switching data via the SSDA every 40ms.

The CPU generates pulses at 8ms intervals to verify that the correct output value has been latched into the Analog Interface comparators. These pulses are allowed to pass into guard only if the SSDA verifies that the analog switching data is being transferred normally at 40ms intervals. Once in

guard, the pulses prevent the watchdog flip-flops from generating their four BARK and BARK DELAYED output signals; by re-triggering a monostable (M10-4 : 18ms).

If two or more pulses are missing, M10 releases the hold, and the watchdog flip-flops 'Bark', activating the safety circuitry. They will be missing if the output value comparators are incorrectly updated, or if the SSDA fails to generate 'Transmit' IRQ pulses for a period exceeding 470ms, or if the CPU crashes.

The in-guard watchdog circuits are located on the Referece Divider pcb; the out-guard control signals originate in the Digital pcb and are processed in the Analog Interface pcb.

4.5.6.1 Out-Guard Watchdog
(Circuit Diagrams 430570 Section 7.3 and 430535 Section 7.4)

The CPU verifies the validity of each serial-interface transfer by instructing the SSDA to generate a 'Watchdog Enable' trigger. This pulse, termed W.DOG ENBL SET (M44-7 on p7.3-3), triggers watchdog-enabling monostable M29-11 (p7.3-1).

W.DOG ENBL SET triggering and retriggering extends the natural (470ms) unstable state of M29 indefinitely. Unless the retriggers fail, W.DOG ENABLE at M29-9 remains at logic-Ø. Absence of W.DOG ENBL SET retriggers for longer than 470ms allows M29-9 to restabilize to logic-1.

W.DOG ENABLE is inverted at M43-3 and applied to NAND M46-12 (p7.3-4).

During each successful processor cycle, the CPU addresses M51-9 (Digital Assembly p7.2-2). The resulting low active pulses at 8ms intervals are inverted, and gated with WRT STRB to generate the active-low signal W.DOG at M49-11.

W.DOG travels via the Mother Assembly to the Analog Interface Assembly where it is gated with the W.DOG ENABLE signal at NAND M46 (p7.3-4). The resulting signal at M46-13, W.DOG, consists of positive-going pulses at 8ms intervals when the CPU/SSDA system is working normally, or a logic-1 level if the SSDA fails.

The W.DOG signal travels via the Mother Assembly to be passed into guard on the Reference Divider Assembly (Opto-coupler M9 on p7.4-5).

4.5.6.2 In-Guard Watchdog
(Circuit Diagram 430535 Page 7.4-5)

NOTE: The operating levels of the in-guard CMOS circuits are negatively displaced as follows (nominal voltages):

Opto-coupler output circuits
- logic-1: -10Vdc
- logic-Ø: -15Vdc

Digital CMOS circuits
- logic-1: 0V
- logic-Ø: -15Vdc

Level-shifter M36 carries out the interfacing between these two levels.

The signal, W.DOG, is opto-coupled into guard by M9. During normal operation the W.DOG in-guard positive-going 8ms pulses trigger and successively re-trigger the monostable M10-4 to give a continuing logic-Ø at M10-7. The 18ms unstable state of the monostable allows for the absence of one pulse, but the absence of two or more pulses allows M10 to reset, taking M10-7 to logic-1.

The logic level from M10-7 is applied to the set input of flip-flop M13-6. With reset M13-4 at logic-Ø during normal operation, the output conditions of M13-1 and M13-2 are as follows:

(1) Set input M13-6=logic-Ø (no fault);
M13-1 (Q)=logic-Ø — BARK not active
M13-2 (Q)=logic-1 — BARK not active

(2) Set input M13-6=logic-1 (malfunction);
M13-1 (Q)=logic-1 — BARK active
M13-2 (Q)=logic-Ø — BARK active

The action of M13-2 changing to logic-Ø, triggers monostable M10-11 which has a relaxation time of 47ms. After 47ms, M10-9 output clocks flip-flop M13-11 to give the command BARK DEL from M13-13 and BARK DEL from inverter M14-12.

4.5.6.3 Power-On Reset (Circuit Diagram 430535 Page 7.4-5)

When power is first applied, the build-up of the -15V supply forces shift register M37 Set inputs to logic-Ø, but its Reset inputs are held at logic-1 by the charging action of R122/C7.

So M37 is forced into reset state for about 80ms:
M37-2 imposes logic-1 at M13-8 Set input.
M37-1 at logic-Ø holds M10 inactive at M10-3, thus preventing random triggering at M10-4 from erratic W.DOG inputs, as the SSDA/CPU functions start up. 'Q' output M10-7 holds M13-6 Set input at logic-1.

Also, the Reset inputs M13-4 and M13-10 are held at logic-1 for a period of 470ms from power-on by the signal FP RST, generated by the power-on reset action of M53 on the Digital Assembly (p7.2-2).

Therefore, the Set/Reset inputs M13-8/M13-10, initially both at logic-1, force M13-13 output to logic-1 to give active BARK DELAYED and BARK DELAYED outputs.

The Set/Reset inputs M13-6 and M13-4, also initially both at logic-1, force:
M13-1 to logic-1 (Active BARK), and
M13-2 to logic-1 (Non-active BARK).

The output conditions of M37 (M37-1=logic-Ø, M37-2=logic-1) remain unchanged after the 80ms time constant at M37 Reset inputs, but then M37-11 is free to be triggered from the SSDA strobe input. Two strobe inputs must occur before M37-1 clocks to logic-1 and M37-2 to logic-Ø. M13-13 now changes to logic-Ø, making BARK DELAYED and BARK DELAYED inactive, and the inhibit is removed from M10-3.

The outputs M13-1 and M13-2 remain unchanged until M10-7 fals to logic-Ø by the clocking action of pulses on the W.DOG input. This must occur before M13-4 returns to logic-Ø (at 470ms from power-on) for BARK to be made inactive, otherwise BARK remains active and BARK is set to logic-Ø, giving a fail status bit to the CPU.

4.5.6.4 Malfunction (Fig 4.5.4)

Any malfunction which introduces one of the following conditions will cause the watchdog to bark:

a. CPU WRT STRB fails at logic-Ø.
b. M51 on the Digital Assembly does not receive the address to activate M51-9.
c. The SSDA fails to transmit bursts of the W.DOG ENABLE SET pulses to M29 (SSDA is not transferring serial data).
d. The SSDA Strobe is not triggering M37.
e. W.DOG pulses are not triggering M10.

In addition to failures at these points, the CPU is informed via SSDA Status byte transfer of certain analog malfunctions. Subsequent CPU action can include deliberate activation of the watchdog by omitting to address M51 as in (b) above.

4.5.6.5 Safety Reset

Once the watchdog has 'Barked' it can be reset, if the malfunction has cleared, by pressing the Safety Reset control on the front panel.

The Safety Reset input to the watchdog circuit, FP RST, is active for 100ms after pressing the Safety Reset key. (M53-9 on Digital Assembly p7.2-2). During this period, the Reset inputs at M13-4 and M13-10 are held at logic-1, allowing the correct pulse inputs from the processor and SSDA to hold M13-6 at logic-Ø, and to reset M13-13 to logic-Ø. The watchdog will not reset if the malfunction persists.

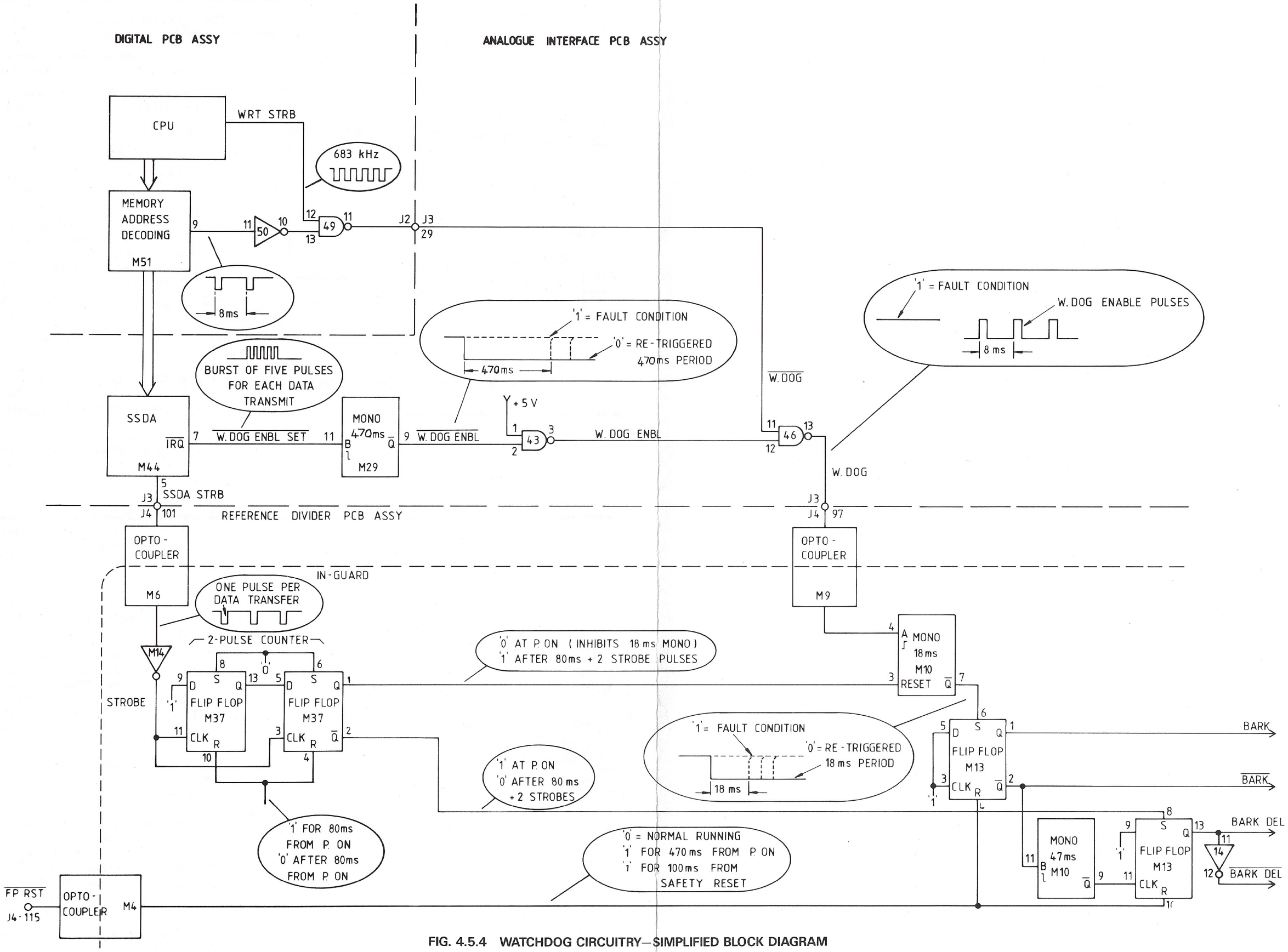


FIG. 4.5.4 WATCHDOG CIRCUITRY—SIMPLIFIED BLOCK DIAGRAM

4.6 PRECISION DIVIDER

The out-guard circuitry described in this section performs the following functions:

(1) Receives and latches the demanded output value from the CPU in the form of a 25-bit word.

(2) Generates a continuous 13-bit up-count from the 1.024MHz Master Clock (8ms count cycle).

(3) Compares the 13-bit count with the 13 most-significant bits of the 25-bit word, generating 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Most Significant' JFET switch in the Reference Divider.

(4) Compares the 12 most-significant bits of the count with the 12 least-significant bits of the 25-bit word, generating, 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Least-Significant' JFET switch in the Reference Divider.

The out-guard circuitry is located on the Analogue Interface Assembly.

The in-guard circuitry performs the following functions:

(5) Provides a Master Reference Voltage (20.6V) which is chopped by the 'Most Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 13 most-significant bits of the 25-bit word. The square-wave is smoothed by a 7-pole Bessel filter, to provice a DC voltage whose value varies directly as the Mark/Period ratio of the MSB square-wave.

(6) Provides a Buffered Reference Voltage (8.83V) which is chopped by the 'Least-Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 12 least-significant bits of the 25-bit word. The square-wave is smoothed by a 3-pole Bessel filter to provide a DC voltage whose value varies directly as the Mark/Period ratio of the LSB square-wave.

(7) Conditions the two DC voltages produced by the 7-pole and 3-pole filters, delivering them via full 4-wire connections to be summed on the AC Assembly as a 'Working Reference Voltage' between 0.126V and 2.79V; whose value is accurately proportional to the value demanded by the CPU's 25-bit word.

(8) Digitally generates a stepped AC reference voltage whose peak value is equal to the DC Working Reference Voltage. This gives the RMS Comparator (described in sub-section 4.14) the considerable advantage of comparing AC sense against AC Reference. (If AC were compared with DC, small DC offsets would magnify and lead to 'DC turnover' errors). The AC waveform is constructed in ten steps by a digitally controlled switching network. It has been given the name 'Quasi-Sinewave'.

The in-guard circuitry is located on the Reference Divider PCB Assembly.

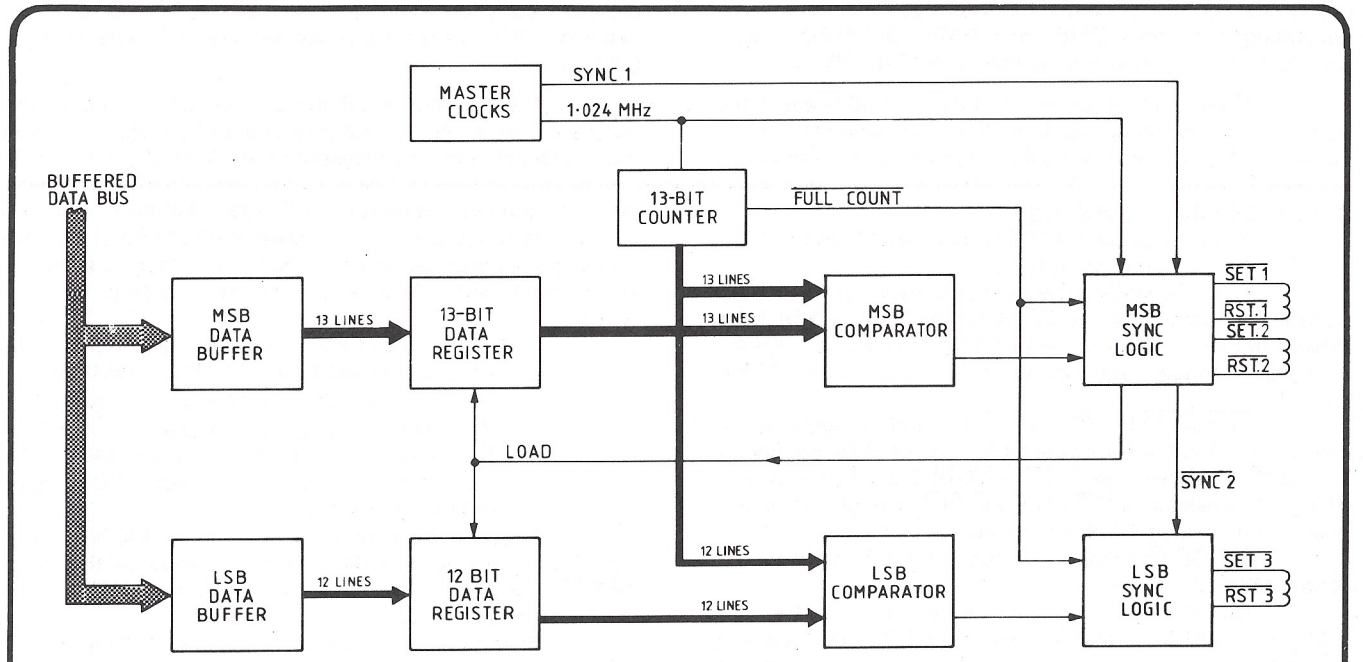


FIG. 4.6.1 PRECISION DIVIDER OUT-GUARD CIRCUITRY—SIMPLIFIED BLOCK DIAGRAM

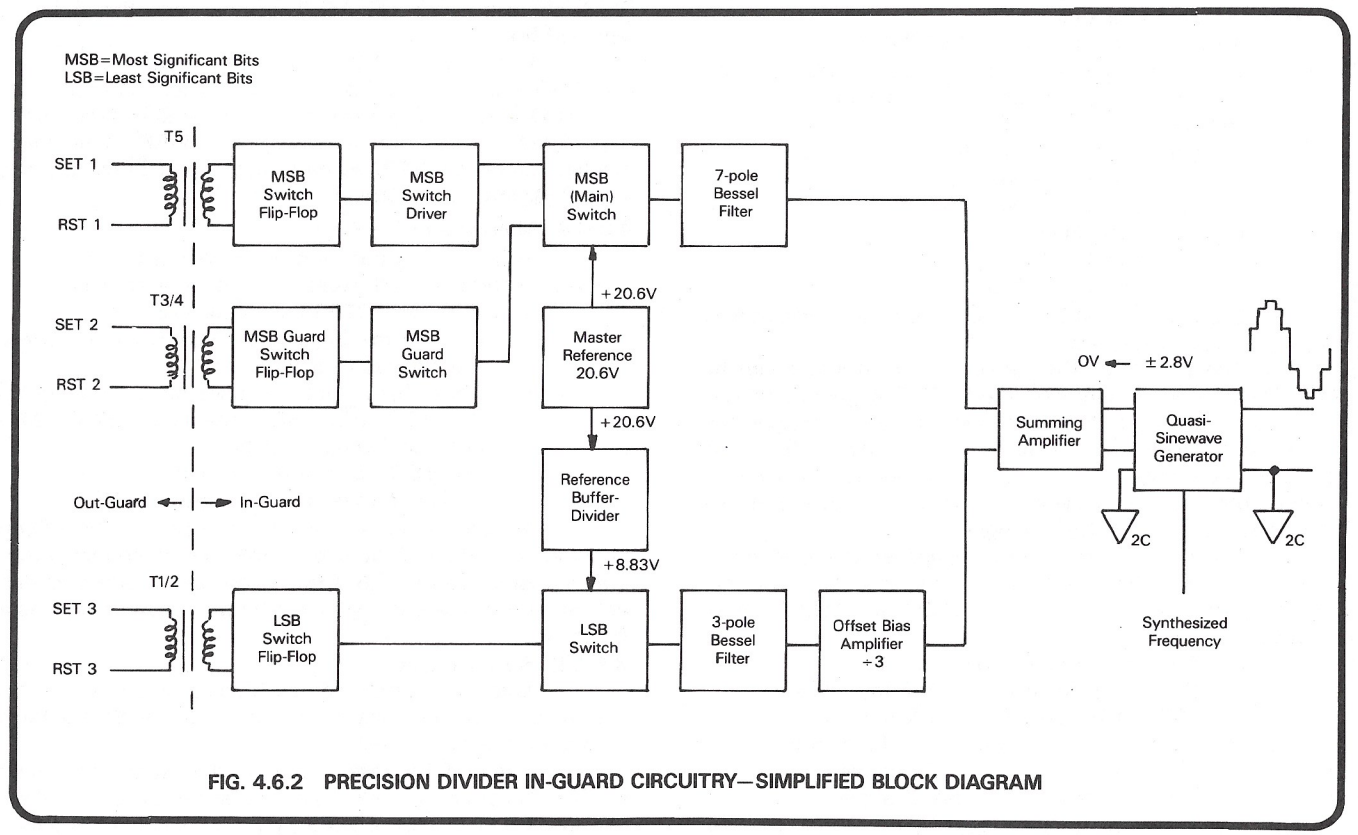


FIG. 4.6.2 PRECISION DIVIDER IN-GUARD CIRCUITRY—SIMPLIFIED BLOCK DIAGRAM

4.6.1 Precision Divider Comparators
(Circuit Diagram No. 430570)

4.6.1.1 General (Figs. 4.6.1 and 4.6.2)

The comparators are designed as a means of translating a binary word into the accurately defined Mark/Period ratio of a square-wave. The ratio of the square-wave's average value to its peak value subsequently defines the division ratio applied to the Master Reference, and must be adjustable at high resolution.

The required decimal resolution translates into a binary word of 25 bits in length, and each bit needs to exert control of the division ratio.

A single comparator of this length would require more than 30 million clocks to scan, which at sensible clock frequencies would occupy several seconds. To filter out the resultant chopping frequency would require large and expensive components, and force unrealistic operational time-constraints.

In the 4200, by splitting the word into two parts: the 13 most-significant bits (MSB) and the 12 least-significant bits (LSB), a scan-cycling frequency of 125Hz is obtained from a 1.024MHz clock.

Both MSB and LSB comparators are scanned concurrently by the same 13-bit counter, forming two separate square-waves. These act on two separate reference divider switches and filters to generate two separate DC voltages which are subsequently recombined in the AC Assembly.

In summary, the two comparators translate information from the CPU into time-related pulses which control mark/period switching in the reference divider. One comparator translates the 13 most-significant bits of CPU data; the other, the 12 least-significant bits. The comparators perform concurrently, cycling continuously at 125Hz, taking 8ms per full count.

At the start of each 8ms counting period, each comparator generates a SET pulse to start its reference divider 'Mark'. Then after precisely-measured delay times, each generates a RESET pulse to terminate the 'Mark', and start the 'Space'.

At each 8ms full-count, the clock resets and continues up-counting from zero.

4.6.1.2 Comparator Operation (Fig. 4.6.1)

The MSB and LSB Data Buffers are periodically loaded and latched with binary 'Demanded Output Value' data under the control of the CPU.

At the end of each comparator counting cycle, the 13-bit counter $\overline{\text{FULL COUNT}}$ output enables the generation of set pulses $\overline{\text{SET 1}}$, $\overline{\text{SET 2}}$ and $\overline{\text{SET 3}}$ by the MSB and LSB 'Sync Logic' circuits.

$\overline{\text{FULL COUNT}}$ also generates the LOAD command. This writes the data, currently latched in the buffers, into working data latches which form the 13-bit and 12-bit Data Registers, updating the earlier 'Demanded Output Value' priming the comparator.

The MSB and LSB comparators translate this binary data into 'RESET' pulses, whose time relationships to the 'SET' pulses are established by the value of their binary words.

4.6.1.3 13-Bit (MSB) Comparator
(Circuit Diagram No. 430570 Page 7.3-2)

The 13 binary outputs of the up-counter scan the 13 Exclusive-OR elements of the MSB Comparator. With the least-significant bit at 512kHz, and the most-significant at 125Hz, the 8ms scan time thus divides into 8192 time elements, each of 977ns.

Each time element has a unique binary code, incrementing by one bit on its predecessor. When this coincides with the bit-pattern set in the data register, the comparator provides an output pulse to the MSB sync logic. The latter generates reset pulses $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ in synchronism with the signal SYNC 1 (2.048MHz).

4.6.1.4 12-Bit (LSB) Comparator
(Circuit Diagram No. 430570 Page 7.3-1)

This functions in the same manner as the MSB comparator, but only 12 bits are scanned over the same 8ms counting period. This accomodates 4096 time elements of 1954ns for each binary increment.

SYNC 2 pulses, generated in the MSB Sync Logic circuitry at half the rate of SYNC 1, synchronize the $\overline{\text{RST3}}$ output from the LSB Sync Logic.

4.6.2 Comparator Circuit Action

4.6.2.1 Input Data Latches
(Circuit Diagram 430570 Pages 7.3-1 and 7.3-2)

The input buffered data latches M31 to M34 and M37 to M39 receive 27 data bits in four bytes from the buffered data bus. Latches are selected by signals REF DIV 1, 2, 3 or 4 from the memory address decoding on the digital pcb. Data is clocked to the 'Q' outputs of the latches on the positive-going edge of $\overline{\text{WRT STRB}}$.

Data from the input latches is used as follows:

25 bits form a data word to the comparator registers M47, M48, M49 (part), M51 and M52. One bit triggers monostable M29 (part), the Q output of which is inverted and buffered to provide the control $\overline{\text{UPD (OG)}}$ used in the relay drive logic for analog switching. One bit, EXT FREQ divided by 10, is not used in the 4200.

4.6.2.2 13-Bit Counter

(Circuit Diagram 430570 Page 7.3-2)
(Refer to Fig. 4.6.3 for Waveforms)

The counter comprises three 4-bit binary counters M15, M16, M17 and J-K flip-flop M42 (half dual package). The squarewave outputs from the counter are on 13 binary-coded lines, the first (least-significant) being a 512kHz squarewave, the others successively divided in frequency to the most significant output of 125Hz.

Bit 1 is provided by J-K flip-flop M42, which toggles on each falling edge of the 1.024MHz clock to give 512kHz Q and $\overline{Q}$ outputs. These outputs are used as follows:

(1) Q and $\overline{Q}$ complementary outputs together provide the least-significant input to the 13-bit comparator;

(2) The Q output controls the counting rate of M15, synchronizes M16 and M17, and is used in the gating of $\overline{\text{FULL COUNT}}$.

Counters M15, M16 and M17 are cascaded as a 12-bit counter and synchronously clocked by the 1.024MHz. M15 counting is enabled only when M42 Q output is logic-1 at the count-enable input M15-7.

As M42 output is at 512kHz, clocking of M15 occurs on the rising edge of alternate 1.024MHz clocks, thus giving outputs of 256, 128, 64 and 32kHz squarewaves from M15.

Counter M16 is enabled by the carry output from M15 together with 512kHz from M42 at the count-enable pins M16-10 and 7 respectively, thus giving outputs of 16, 8, 4 and 2 kHz squarewaves from M16.

Counter M17 functions in a similar manner to give outputs of 1kHz, 500, 250 and 125Hz squarewaves.

The 2μs-long carry output from M17 occurs at the end of the 125Hz output when all counter outputs are at logic-1. The carry output is NANDed with M42 Q output to give the 1μs-long logic command $\overline{\text{FULL COUNT}}$. The counting cycle resets and continues, starting from bit 1.

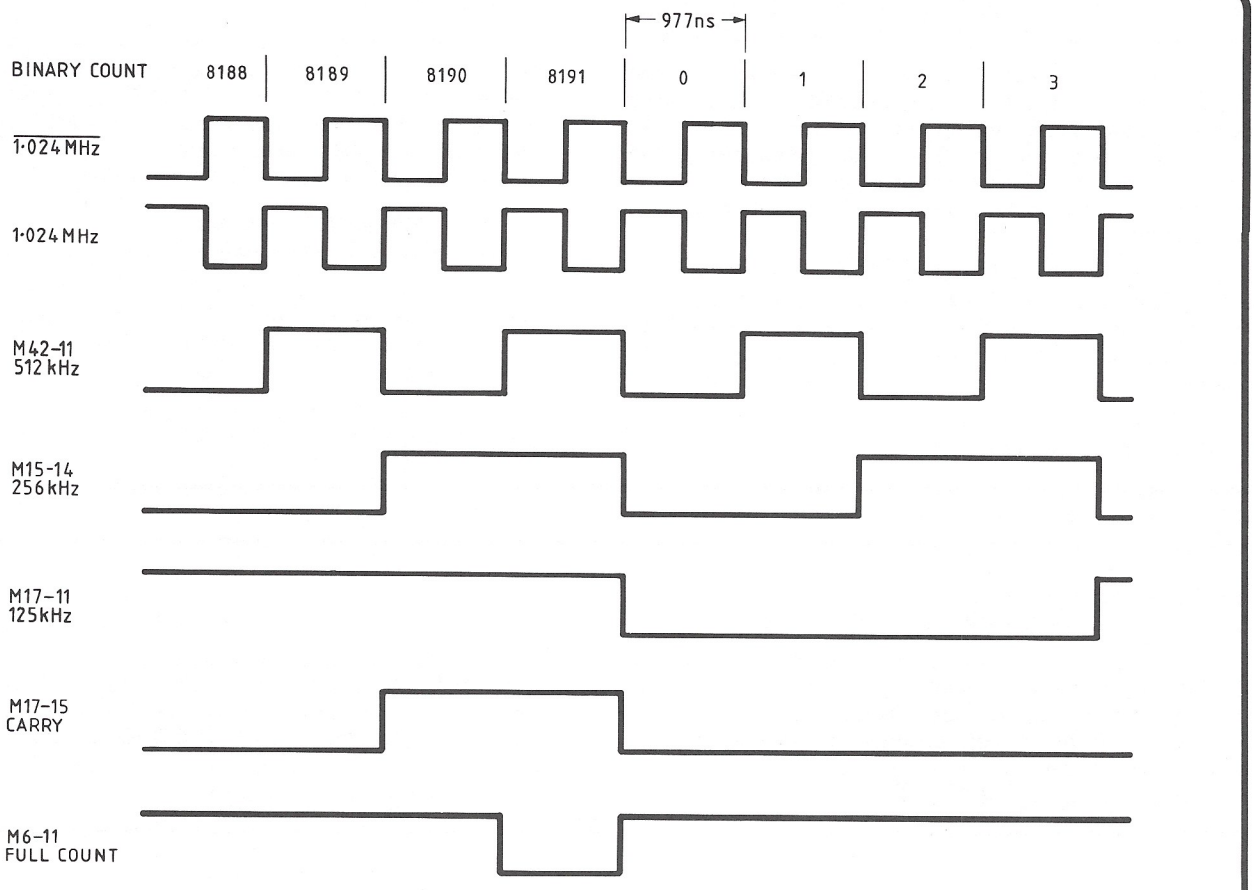


FIG. 4.6.3 13-BIT COUNTER WAVEFORMS

4.6.2.3 13-Bit Comparator Action
(Circuit Diagram 430570 Page 7.3-2)

The 13-bit comparator provides a logic-1 output at TP12 whenever a coincidence occurs between the following two sets of data:

(1) Data set in registers M47, M48 and M49-1;

(2) Data from 13-bit counter M42, M15, M16 and M17.

Twelve exclusive-OR elements M25, M26, M27 and three NOR gates of M12 are used to detect a coincidence. The data in the registers is preset by the CPU, while that presented by the 13-bit counter cycles through every binary combination possible on 13 lines.

Two coincident inputs to an exclusive-OR gate provide a logic-Ø to the 12-input NOR gates M24/M23; full coincidence in bits 2 to 13 is shown by a logic-Ø at NAND M13-6. Coincidence at bit 1 is shown by logic-Ø at M12-13 and M12-4 as follows:

M12 INPUT PINS			M12 OUTPUT PINS		
6	11	9/12	4	13	
0	1	0	0	0	only 4 input combinations available
0	1	1	1	0	
1	0	0	0	1	
1	0	1	0	0	

A $\overline{\text{BUSY}}$ signal is generated by the comparator at NAND M50-13 (TP2) when the 13-bit counter approaches full count. Bits 8 to 13 are at logic-1 for the period of 125μs preceding the end of the counter cycle (see Fig. 4.6.4). The $\overline{\text{BUSY}}$ level is applied to the D input at M49-9 and is synchronously clocked through as $\overline{\text{REF BUSY}}$ to buffer M45-2 by 1.024MHz.

As described earlier, the demanded output value is defined by the CPU to a resolution of 25 bits, contained in four data bytes. The time needed for the 4-byte transfer could allow the latches to contain spurious data until they were fully loaded, and an inaccurate parity could be registered with the counter still running. The counter must not be interrupted, as its full count defines the 'period' of the mark-to-period ratio, which is used to control the division of the reference voltage. It is therefore necessary to reduce the loading time, and this is achieved by double-latching the data.

When the CPU has data to load into the input data latches, it first interrogates the comparator by enabling buffers M45 through $\overline{\text{REV DIV RD}}$. The $\overline{\text{REF BUSY}}$ signal at logic-1 (M45-3) indicates to the CPU that sufficient time is available for the latch-loading process to take place (at least 125μs remain before the LOAD pulse occurs).

If the $\overline{\text{REF BUSY}}$ signal is at logic-Ø, the CPU waits until it returns to logic-1 again.

When the $\overline{\text{REF BUSY}}$ signal is at logic-1, the CPU loads the data by first carrying out four transfers of one byte each into the seven quad buffer latches M31 to M34, and M37 to M39. Each byte's destination is addressed by one of the chip-select signals $\overline{\text{REF.DIV.1}}$ to $\overline{\text{REF.DIV.4}}$, which enables the selected buffer latches. The data is latched by the $\overline{\text{WRT STRB}}$ signal.

Once the full 25-bit word has been latched into the buffers, it is available as a single word at the data inputs of the comparator latches M47, M48, M49, M51 and M52. The CPU again interrogates the comparator by $\overline{\text{REF DIV RD}}$, and five of the elements of M45 buffer the five most-significant data bits back to the CPU.

If parity with the transmitted data is confirmed, the CPU takes no action. When the counter times out, the $\overline{\text{FULL COUNT}}$ signal is clocked through to M14-6 by $\overline{\text{SYNC 2}}$ as the LOAD signal, and the new data is transferred into the comparator latches.

If the data latched in the buffers is not as transmitted, the CPU initiates the FAIL 4 message procedure to the operator.

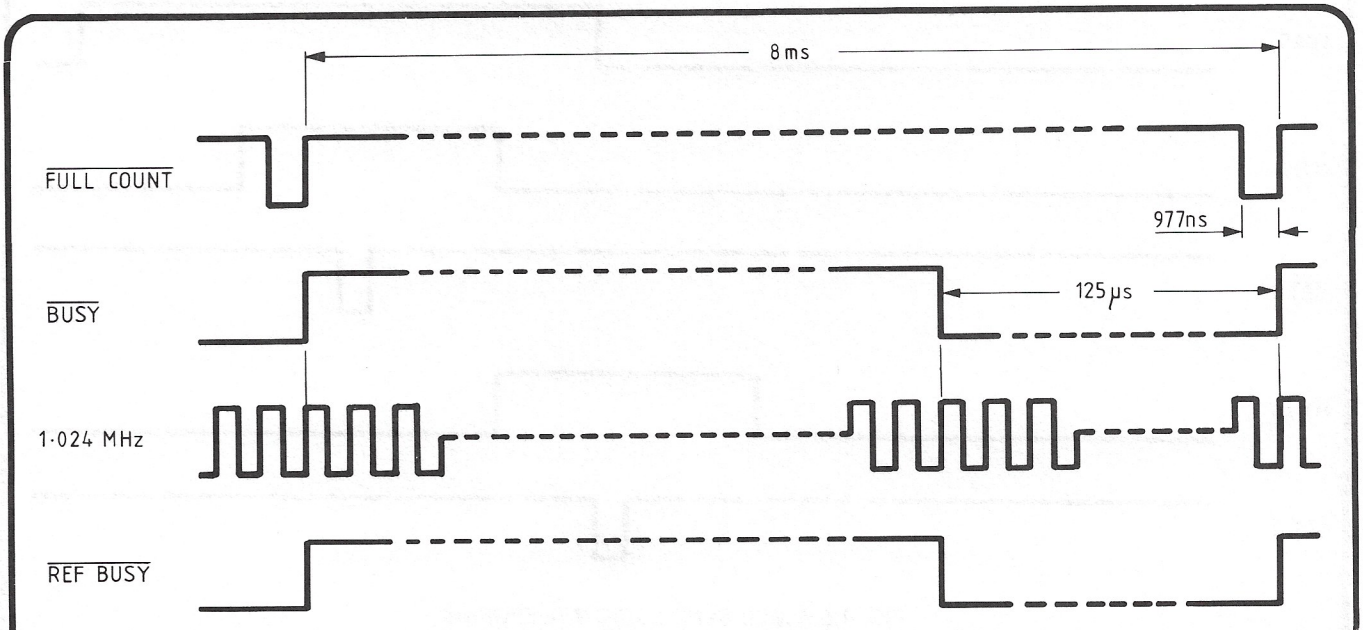


FIG. 4.6.4 BUSY WAVEFORMS

4.6.2.4 'Most Significant Bits' SYNC Logic

(Circuit Diagram 430443 Page 7.3-2)
(Refer to Fig. 4.6.5 for Waveforms)

This circuit, M14, M6, M7 and M8, provides the following signals: $\overline{\text{SYNC 2}}$, LOAD, $\overline{\text{SET 1}}$, $\overline{\text{SET 2}}$, $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$.

$\overline{\text{SYNC 2}}$ is obtained by NAND gating 1.024MHz and SYNC 1 to give a synchronizing pulse at half the rate of SYNC 1. (See Fig. 4.6.5).

The LOAD pulse enables the 13-bit comparator registers, and is generated at M14-6 towards the end of the counter's full-count output. $\overline{\text{FULL COUNT}}$ sets the D input M14-2 and the level is clocked, inverted, from M14-6 by the next two $\overline{\text{SYNC 2}}$ pulses that occur.

The inverse of LOAD is used to time the pulse $\overline{\text{SET 1}}$ by NOR gating at M7-4 with 1.024MHz. The pulse at M7-4 is then NAND gated with SYNC 1 to provide $\overline{\text{SET 1}}$ from M8-1. The pulse $\overline{\text{SET 2}}$, which occurs 977ns before $\overline{\text{SET 1}}$, is obtained by gating $\overline{\text{FULL COUNT}}$ with 1.024MHz at NOR M7-10 and then NAND gating at M8-10 with SYNC 1.

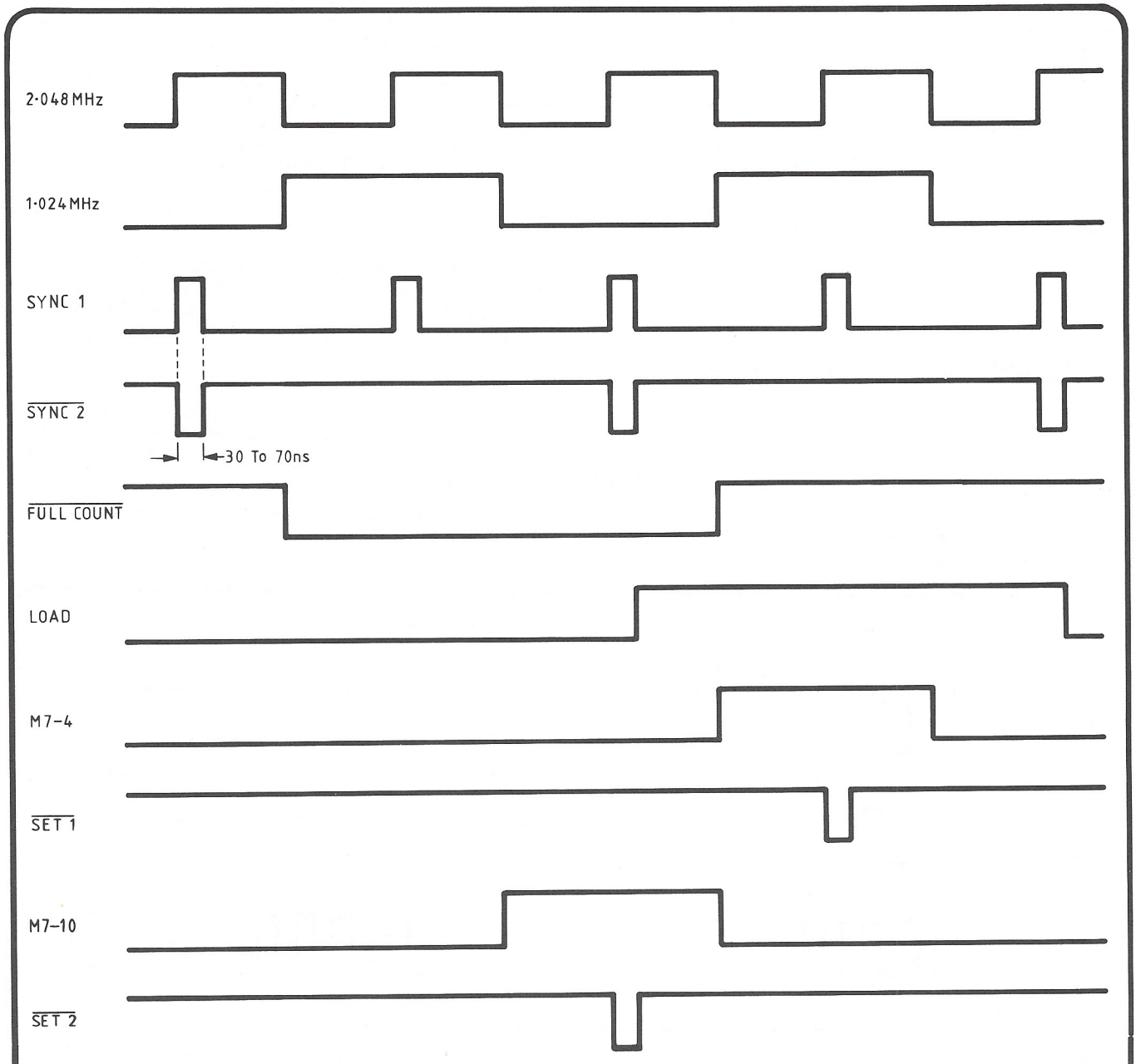


FIG. 4.6.5 MSB SYNC LOGIC WAVEFORMS

Reset pulse generation (see Fig. 4.6.6) is initiated by a logic-1 level at TP12. This can occur at any one of the 8192 binary counts of the 13-bit counter, the actual time slot in which it appears depends on the binary count at which the coincidence occurs.

The coincidence level at TP12 is NAND gated at M6-8; M6-10 being at logic-1 for all binary counts except 8191. The logic-Ø at M6-8 is NOR-gated at M7-1 with 1.024MHz, this is then used to select the next SYNC 1 pulse via NAND M8-4 to provide the pulse $\overline{\text{RST 1}}$.

The coincidence level at TP12 is used to set the D input at flip-flop M14-12. This level is clocked to NAND M6-5 by the next $\overline{\text{SYNC 2}}$ pulse. NAND input M6-4 is at logic-1 except when LOAD is active, thus M14-9 output is inverted at M6-6 to be NOR-gated with 1.024MHz at M7-13. This is then used to select the next SYNC 1 pulse via NAND M8-10 to provide the pulse $\overline{\text{RST 2}}$.

The pulse-timing example given in Fig. 4.6.6 shows the generation of $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ when coincidence occurs in the comparator at binary count = 0 (waveforms in continuous lines).

Coincidence occurring at binary count 1 causes $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ to increment in time by 977ns with respect to the $\overline{\text{SET 1}}$ and $\overline{\text{SET 2}}$ pulses (waveforms in broken lines).

$\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ are generated with the same relationship in time to the comparator coincidence when the latter occurs in any binary count time slot from 0 to 8190 (inclusive).

Note that as the comparator word increments in value, $\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ increment in time after $\overline{\text{SET 1}}$ and $\overline{\text{SET 2}}$, which remain stationary with respect to $\overline{\text{FULL COUNT}}$ and LOAD.

$\overline{\text{RST 1}}$ and $\overline{\text{RST 2}}$ are inhibited when coincidence occurs at binary count 8191 to allow for the re-loading of the input registers at the end of the counter cycle. The inhibit is performed by the $\overline{\text{FULL COUNT}}$ level going to logic-Ø and NAND M6-10 which prevents $\overline{\text{RST 1}}$ being generated, and by flip-flop M14-5 output going to logic-Ø for the period of the load pulse which inhibits $\overline{\text{RST 2}}$.

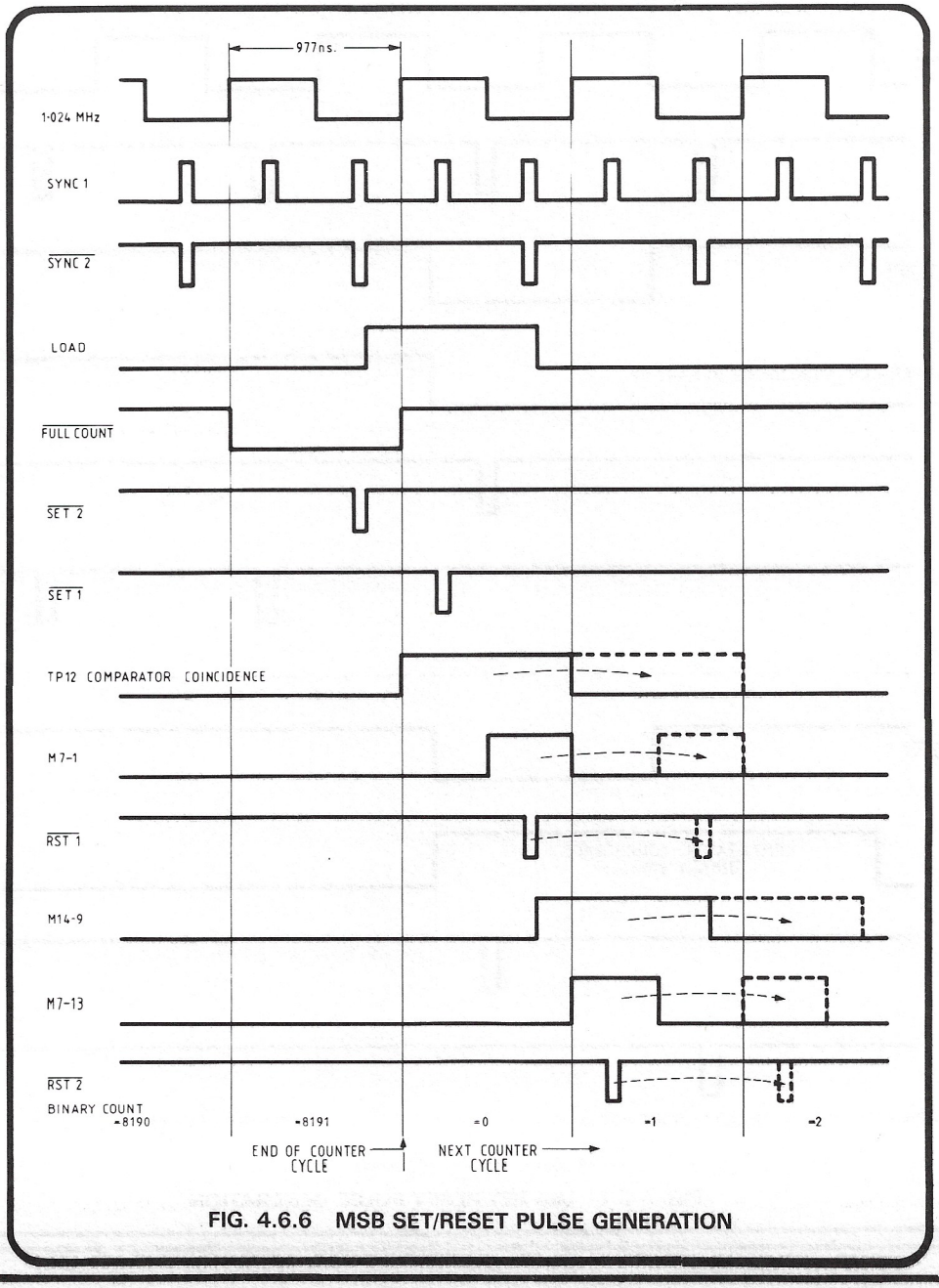


FIG. 4.6.6 MSB SET/RESET PULSE GENERATION

4.6.2.5 12-Bit Comparator Action
(Circuit Diagram 430570 Page 7.3-1)

This functions in an identical manner to the 13-bit comparator previously described. Twelve exclusive OR gates, M19, M20 and M21, receive the 12-bit binary output from the common counter and compare these bits with the data in the data registers. The least-significant bit changes at a rate of 256kHz, and the most-significant bit at 125Hz. Coincidence occurring in any of the 4096 binary-count time slots available in the comparator cycle is shown as a logic-Ø at TP5 for a period of 1954ns.

4.6.2.6 'Least Significant Bits' SYNC Logic
(Refer to Fig. 4.6.7 for Waveforms)

The timing of $\overline{\text{SET 3}}$ is controlled by the $\overline{\text{FULL COUNT}}$ pulse from the 13-bit counter. The inverted $\overline{\text{FULL COUNT}}$ at M43-6 is gated with the inverted $\overline{\text{SYNC 2}}$ from M43-11 to give, at M46-1, $\overline{\text{SET 3}}$.

The comparator coincidence logic level is inverted to logic-Ø at M12-1; M12-2 being at logic-Ø except when $\overline{\text{FULL COUNT}}$ is low. The waveform at M12-1 is of 1954ns duration and therefore allows two consecutive $\overline{\text{SYNC 2}}$ pulses to be gated to M46-4 ($\overline{\text{RST 3}}$).

This condition exists for all $\overline{\text{RST 3}}$ timings except at the binary count of 4095; in this instance, the $\overline{\text{FULL COUNT}}$ pulse occurs after the gating of the first $\overline{\text{SYNC 2}}$ pulse, sets M12-2 to logic-1 and so prevents the second pulse appearing at $\overline{\text{RST 3}}$. In practice, the second pulse of $\overline{\text{RST 3}}$ has no operational significance.

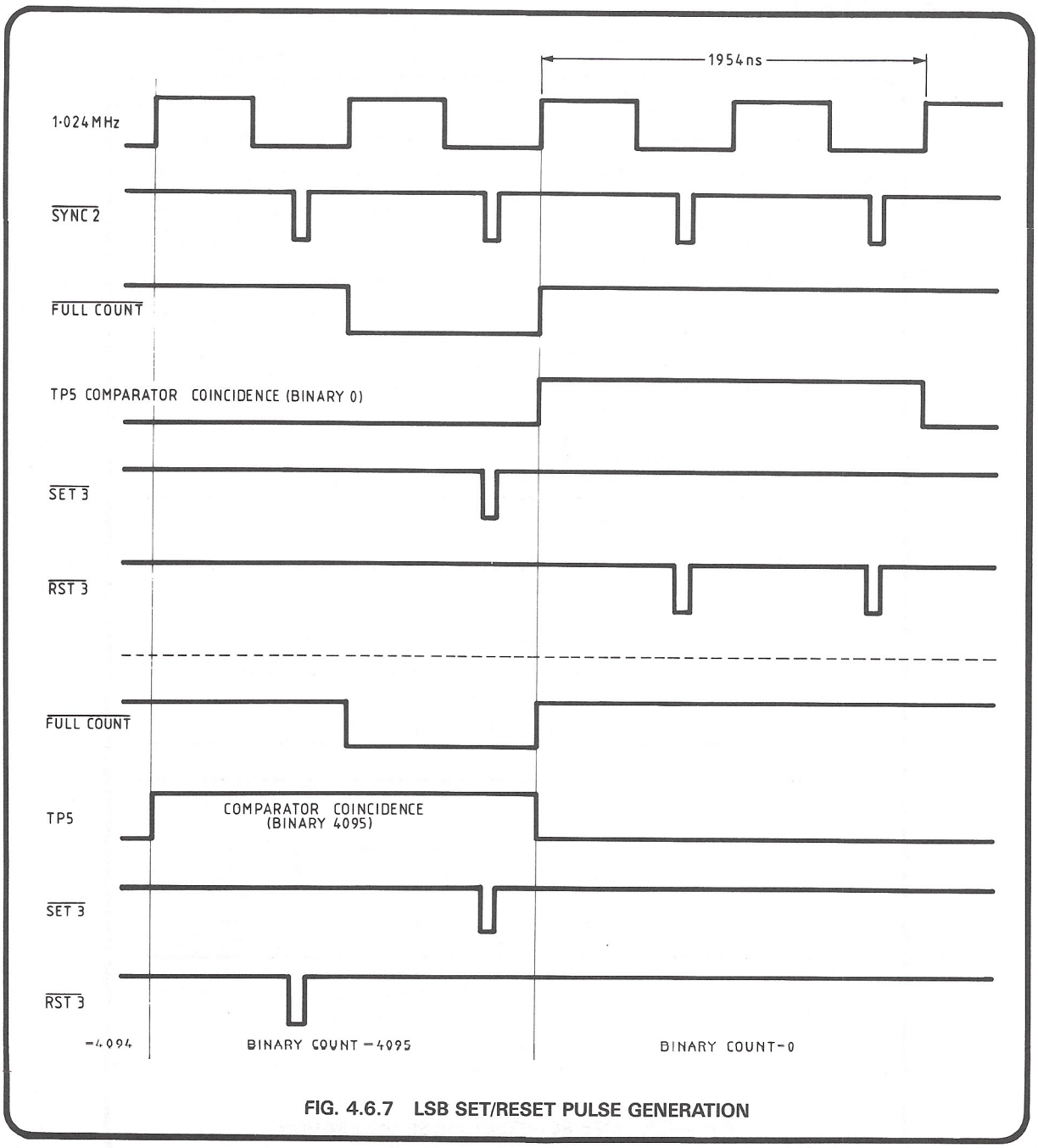


FIG. 4.6.7 LSB SET/RESET PULSE GENERATION

4.6.3 References and Reference Divider

(Circuit Diagrams 430535 Section 7.4)
(Refer also to Fig. 4.6.2)

The set and reset pulses from the precision divider comparators control the timing of JFET switches which chop the Master Reference voltages.

The chopped references are filtered to generate two voltages whose levels are proportional to the MSB and LSB squarewaves' mark:period ratio (duty cycle). These MSB and LSB voltages are conditioned, and transferred to the AC Assembly by full 4-wire sensed connection where they are summed at a star-point to generate a Working Reference: 'REF+Ve'.

REF+Ve is adjustable at high resolution (0.03ppm:approx. 0.6μV increments), with a maximum possible range of adjustment of 0-20V.

The Reference Divider and Master Reference are also employed in other Calibrators of the series, where the high available resolution is advantageous. In the 4200, however, such resolution is not necessary for the 6½-digit accuracies associated with AC outputs. Also, the basic range is the 1V Range, all other ranges employing either attenuation or amplification. The working reference is therefore reduced to 0.126V to 2.79V by software, which results in a reduction of the maximum mark:period ratio of the chopping waveform to about 0.14.

4.6.4 Master Reference

(Circuit Diagram 430553 page 7.4-4)
(Refer also to Fig. 4.6.8)

The Master Reference determines the fundamental long and short-term stability of the 4200. It is a separate pcb mounted on the Reference Divider Assembly.
(Refer to the Layout Drawing facing Page 7.4-7)

The basic circuit shown in Fig. 4.6.8 acts as a constant-current generator for a zener reference.

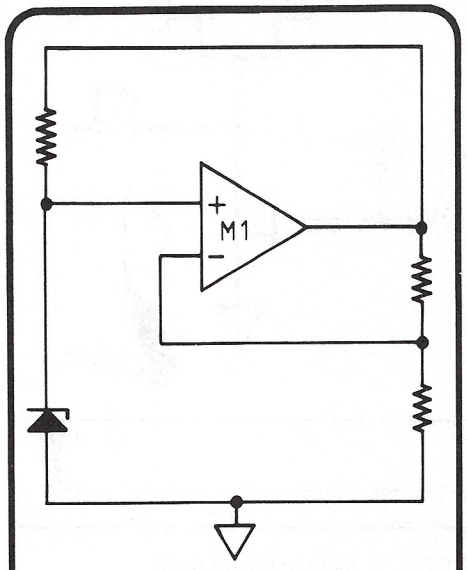


FIG. 4.6.8
BASIC REFERENCE CIRCUIT

The random character of zener drift in the short-to-medium term may in the long term be regarded as averaging to zero. The averaging action of the four zener diodes on Page 7.4-7 reduces the short and medium term variations (due to drift and noise) by a factor of $\sqrt{4}$, effectively twice as stable as a single zener diode.

The diodes and resistors are selected and matched for near-zero temperature coefficient; the overall instrument values are shown together with the stability and accuracy specifications in Section 6 of the User's Handbook.

At manufacture, the zener operating current is adjusted for zero temperature coefficient, by selectively removing links TLA1-5.

The zener voltage of +24.5V at TP3, with respect to Common-R1, is reduced by R24/R25/R26 to +20.6V. This is an approximate value, but it has high temperature and time stability. It is corrected by constants stored in non-volatile memory during calibration. The +20.6V is then buffered by M2 for transmission, at the same value, to the 'Most Significant' Switch in the Reference Divider. Delivery is by sensed connection, the Reference Common-R1 being connected to the Reference Divider Common-4, by a low-resistance wire link from pin A.

4.6.4.1 Buffer M2—Temperature Compensation

(Circuit Diagram 430553 page 7.4-7)

In the 4200 instrument, the temperature compensation applied to M2 is adjusted at manufacture by R29 (set TC slope). This adjustment requires specialised test equipment and should not be attempted by users.

If a fault is suspected on the Reference PCB Assembly (400553), contact your Datron Service Center.

4.6.5 Reference Buffer-Divider

(Circuit Diagram 430535 page 7.4-2)

R80/81 drop the 20.6V Master Reference voltage (V_{Ref}) to +8.83V. M23/Q40 is a voltage-follower providing +8.83V wrt common-4 at the star-point TP11 to supply the least-significant digit switch.

4.6.6 Least-Significant-Digits Switching
(Fig. 4.6.9)

4.6.6.1 Switch Driver

$\overline{\text{SET 3}}$ and $\overline{\text{RST 3}}$ pulses from the LSB Comparator in the Analog Interface Assembly are transferred into guard via pulse transformers T1 and T2, whose centre-tapped secondaries are balanced about Common-4 0V (T1) and +9V (T2).

Q5-Q7 form a fast bistable using emitter-coupled logic, to switch TP1 between +9V (mark) and +20V (space).

During the "Mark" time after SET 3 pulse, Q29 and Q30 are switched ON, connecting LKA to +9V Ref. Q1-Q4 have the same bistable action, switching Q31 off during the "Mark" period by −11V at TP2, thus disconnecting LKA from common-4 (0V).

During the "Space" time after $\overline{\text{RST 3}}$ pulse, Q29 and Q30 disconnect LKA from +9V Ref, and Q1-Q4 switch Q31 on, connecting LKA to common-4 (0V).

Fig. 4.6.9 demonstrates this action.

4.6.6.2 JFET Switch and 3-Pole Filter

The combined action of the switch FETs alternately provides charging current for the 3-pole filter (during 'mark') and discharging current (during 'space').

Two JFETs in parallel (Q29 and Q30) are necessary to equalise the charging and discharging time-constants by matching the "ON" resistances. This preserves linearity of the filter output voltage over the full range of mark/period ratios applied via the set and reset pulses.

The 3-pole filter has the advantage of not being in series with the DC output signal. The 125Hz ripple content is reduced to an acceptable level for the overall instrument specification. The filter output is buffered by voltage-follower M16.

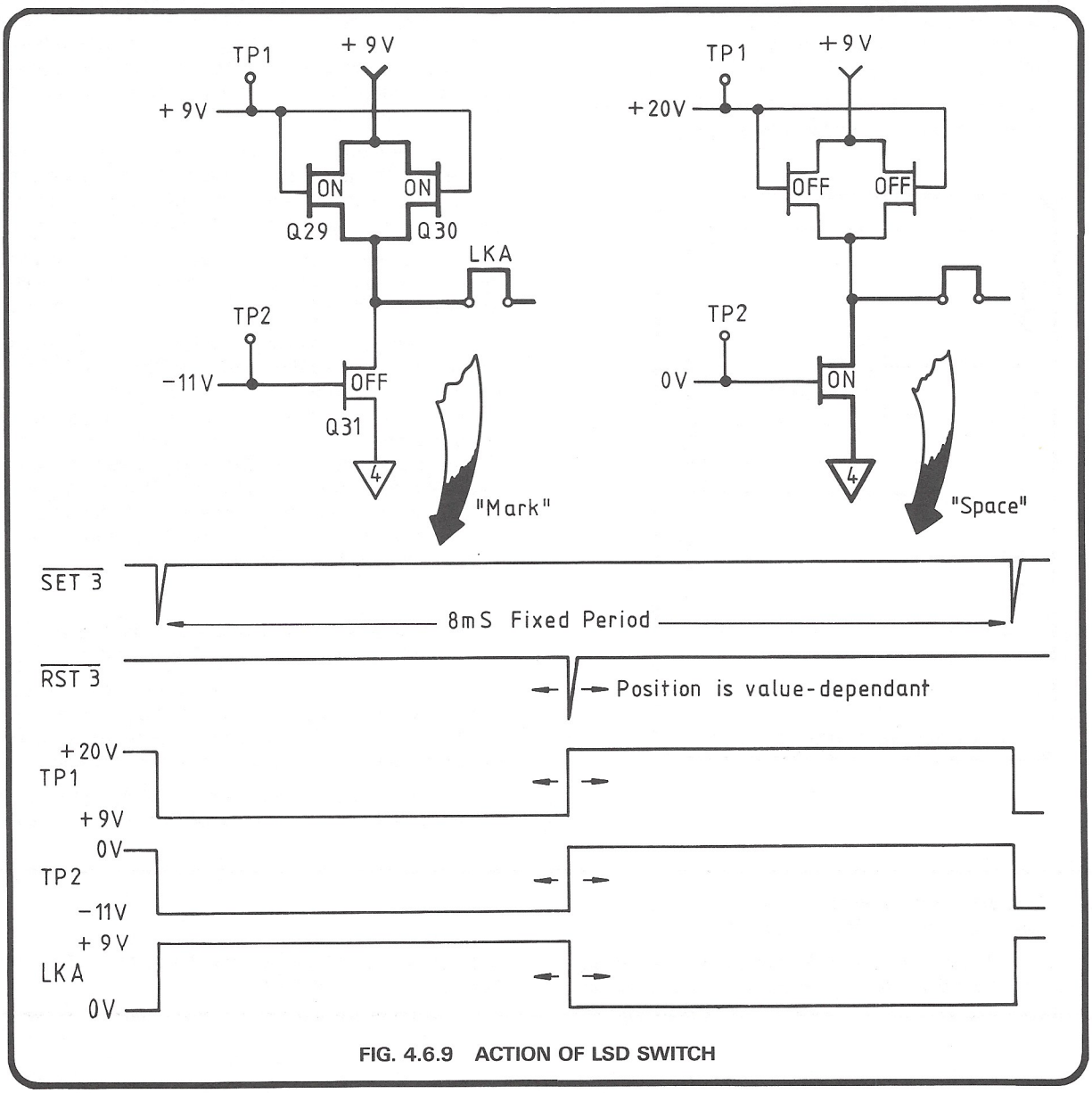


FIG. 4.6.9 ACTION OF LSD SWITCH

4.6.6.3 Offset Bias Amplifier

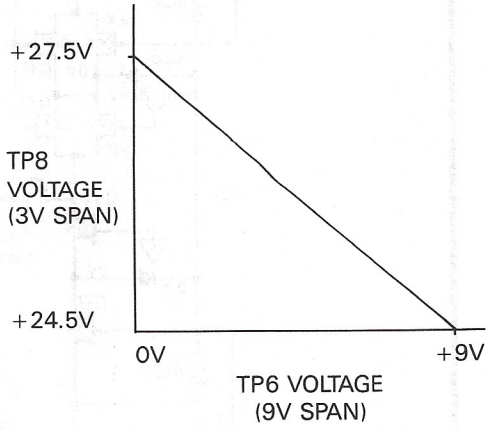
M20 performs a dual role:

(1) Its gain is set to $\frac{1}{3}$ by $\frac{R65}{R64}$

(2) Its output is level-shifted to provide an offset bias for summing (this allows the summed output to have a negative zero offset).

Also a small thermal coefficient zero correction is factory-preset (D10/R85).

M20 transfer function is approximately as follows:



The actual values are as set digitally in software, affecting the mark:period ratio of the JFET switches, using stored calibration constants.

4.6.7 Most-Significant-Bits Switching

(Circuit Diagram No. 430535 Page 7.4-1)

The large reference voltage (20.6V) and the need for higher resolution makes the MSB Switching circuitry more complex than for LSB; but the principle is the same: the set and reset pulse-timing adjusts the mark:period ratio of the square wave fed to the filter.

The arrangement used for the MSB switching satisfies two essential requirements:

(1) The charge and discharge path resistances for the 7-pole filter must be closely matched.

(2) The leakage current of the path switched off must be minimal.

Requirement (1) demands that the matched devices used in both paths are of the same type (P-channel JFETs have approximately 10 times the "on" resistance of N-channel types). But without the voltage standoff and leakage current shunt created by the guard switch, the pinch-off gate voltage for one of the paths would be high enough to generate gate-leakage current in excess of requirements (2).

4.6.8 Main And Guard Switches (Fig. 4.6.10)

(Circuit Diagram 430535 Page 7.4-1)

Refer to Fig. 4.6.10, in which only the Space to Mark (SET) state transfer a-b-c is shown.

(The Mark to Space (RESET) transfer is symmetrical c-b-a)

The switch driver flip-flops establish the voltage shown at TP3, 4 and 5 as controlled by the set and reset pulses. The drivers are ECL fast bistables, but note that Q19 and Q20 are included in the main switch driver as a level-shifter for Q32/Q35.

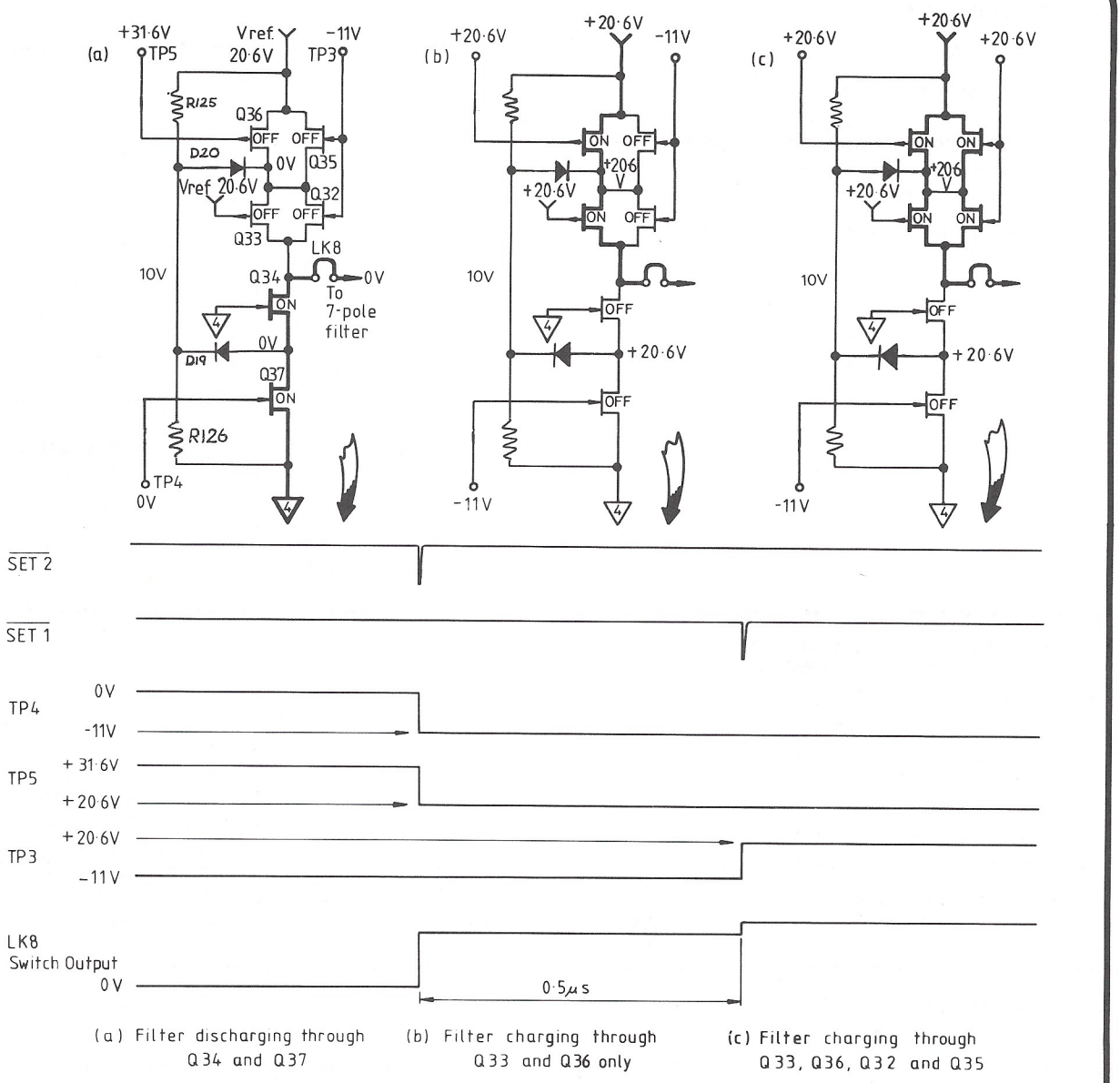


FIG. 4.6.10 ACTION OF MAIN AND GUARD SWITCHES (MSD)

4.6.8.1 Switch Timing
(Fig. 4.6.10)

$\overline{\text{SET 1}}$ pulse is delayed by 0.5μs after $\overline{\text{SET 2}}$ pulse, and $\overline{\text{RST 2}}$ is delayed by 0.5μs after $\overline{\text{RST 1}}$.

$\overline{\text{SET 2}}$ and $\overline{\text{RST 2}}$ pulses control the timing of Q36, Q33, Q34 and Q37 in the main switch (TP4 and 5).

$\overline{\text{SET 1}}$ and $\overline{\text{RST 1}}$ pulses turn Q35 and Q32 on and off (TP3). Because of the 0.5μs delays, Q35 and Q32 conduct only during the time that Q36 and Q33 are also conducting.

4.6.8.2 Filter Discharge Path

In Fig. 4.6.10(a) the switches are in "space" state:

Q37 and Q34 are turned on by TP4 at OV, to provide the filter discharge path.
Q33 and Q36 are turned off by TP5 at +31.6V,
Q32 and Q35 are turned off by TP3 at −11V.

The filter discharges via resistor R79 and FETs Q34 and Q37. During both Mark and Space periods, R79 (78.7kOhms) is a major determinant of the 7-pole filter charge and discharge currents. Because in 'space' state the 'On' resistances of Q34 and Q37 (3-5 Ohms each) are very small in comparison, the potential at link B can be regarded as zero when considering the effects of the other switching voltages.

Reverse leakage currents in JFET junctions are normally of the order of a few picoamps unless the junction voltages are much in excess of 20V. To control leakage effects from the four JFETs which are turned off, the cathode of diode D20 is connected to the common junction of the four devices. Its anode is returned to the junction of R125 and R126, close to +10V.

The reverse leakage characteristics for a J108 FET (Q35 and Q32) are generally several times heavier than for a J174 (Q36 and Q33). This means that in this switch, the leakage currents via Q35 and Q32 out of the common junction are 4-5 times greater than those entering via Q36 and Q33.

The net leakage out of the junction holds D20 slightly in forward bias, so that its cathode cannot rise above about +10.3V, when the four FETs are turned off in 'space' state. Thus D20 guards the 'buffer' FETs Q33 and Q32 from the effects of the relatively high voltage on Q36 gate. The effects of the buffer FETs' own leakages on the voltage at the filter input can be regarded as negligible, because Q33 leakage currents towards LKB are virtually balanced by those away via Q32.

4.6.8.3 Filter Charge Path

To preserve linearity over the full range of Mark:Period ratios, the filter charging path time constant must closely match that of the discharge path. Q35 and Q32 are factory-selected to form a matched set with Q34 and Q37, all J108 N-channel FETs (The 'on' resistance of P-channel FETs in a true complementary switch would be much higher: 30-40 Ohms). Nevertheless, to avoid high voltages being developed across Q35/Q32 when changing between states (causing excessive leakage), P-channel FETs are employed. Q36/Q33 are switched on before (and switched off after) Q35/Q32.

Fig. 4.5.10(b) shows this intermediate state after $\overline{\text{SET 2}}$ and before $\overline{\text{SET 1}}$, and Fig. 4.6.10(c) shows the fully-conducting state after $\overline{\text{SET 1}}$. Note that for descriptive purposes, the second step on LKB waveform is heavily exaggerated, and is not readily viewed on an oscilloscope. The slightly longer charging time-constant during this half micro-second, due to the higher resistance of Q36/Q33, is not sufficient to disturb the linearity of the filter in excess of specification.

The voltage between TP4 and LKB during 'mark' state is some 31 volts. In the absence of D19, an adverse voltage distribution could cause excessive reverse leakage in Q37. D19 controls the distribution by limiting the voltage at its cathode to about +10V, constraining Q37 source-gate voltage to a tolerable 20.5V.

4.6.9 7-Pole Filter

(Circuit Diagram 430535 Page 7.4-1)

M26, M28, M32, Q41 and Q42, together with associated capacitors and resistors, form a 7-pole Bessel filter in three active elements; providing approximately 135dB of attenuation at the 125Hz switching frequency and increasing at a rate of 140dB/decade. This allows sufficient bandwidth to avoid excessive settling time while reducing the output ripple to within instrument specification. Q41 and Q42 source-followers provide input bias currents for M26 and M28 from the 15V supplies, and buffer the line from bias-current effects. M32 bias-current effects are insignificant.

The filter output at TP13 is fed to a buffer amplifier as '+Ve SUMMING AMP', to be subsequently added to the output from the Least-Significant Switch offset-bias amplifier. R101 and C51 prevent spikes from the chopper-stabilized buffer amplifier being fed back into the filter.

4.6.10 Summing Amplifier

(Circuit Diagram 430535 Page 7.4-3)

4.6.10.1 '+VE SUMMING AMP' Buffer

M33, M34 and Q44 buffer the '+Ve SUMMING AMP' voltage output from the 7-pole filter (this is proportional to the Mark/Period ratio of the 13 most-significant bits of the binary word which defines the instrument output value demand).

M33 is a high-gain, chopper stabilized integrator with a bandwidth of approximately 10Hz, and Q44 provides additional bandwidth for rejection of HF common-mode noise.

M35, D14, D15, Q48 and Q49 generate boot-strapped supplies to preserve full dynamic-range linearity. Q46 and Q47 establish 3mA constant-current drives for D14 and D15.

The whole amplifier acts as a voltage-follower, M34/Q45 providing the output drive, buffering the output of M33 and Q44. The output is delivered as 'Hi O/P' to the AC Assembly via RL2 (RL1 being permanently de-energized in the 4200). The output is sensed in the AC Assembly to account for the volts-drops in the connecting circuit. The sense feedback voltage 'Hi SENSE' is applied to the inverting input of the whole buffer via R98.

For a zero count in the MSB comparator, the filter output voltage is approximately +3.2mV, and a full count of 8191 would produce +20.6V. These are the voltages which are developed at the buffer output.

4.6.10.2 '–VE SUMMING AMP' Buffer

M38, M39 and Q51 buffer the '+Ve SUMMING AMP' voltage output from the Offset Bias Amplifier derived from the 3-pole filter (this is proportional to the Mark/Period ratio of the 12 least-significant bits of the binary word which defines the instrument output value demand).

The dynamic range of the filter output voltage was originally defined by the Reference Buffer (8.83V) for efficient operation of the FET switching circuitry.

It was scaled in the Offset Bias Amplifier to give +27.5V for an LSB comparator count of zero (from approx. +1.1mV at TP6), and +24.5V for a full count of 4095 (from +8.83V at TP6). It now needs to be scaled down so that its proportionality to the '+Ve SUMMING AMP' dynamic range is correct.

R99 and R100 attenuate the '–Ve SUMMING AMP' input voltage by a factor of 0.8545×10^{-3}. At zero count, +27.5V is reduced to +23.5mV, and at full count +24.5V reduces to +20.9mV. These are the extremes of voltage developed at the buffer output.

The whole amplifier acts as a voltage-follower, but without bootstrapped supplies (the small input voltage dynamic range of approx. 2.5mV does not warrant it). Otherwise the circuit is identical to the '+Ve SUMMING AMP'. M39/Q52 provide the output drive, buffering the output of M38 and Q51. The output, 'Lo O/P', is delivered via RL2 to be sensed in the AC Assembly. The sense feedback voltage 'Lo SENSE' is applied to the inverting input of the whole buffer via R127.

4.6.10.3 Summing

On the AC Assembly, the outputs from the two buffers are summed by defining the 'Lo O/P' level as 'Reference Common' (Common 2C), and the 'Hi O/P' level as 'REF +Ve'. Thus the voltage at 'REF +Ve' with respect to 'Reference Common' will always be 'Hi O/P' minus 'Lo O/P' at their current values.

The reference voltages and reference division circuitry are chosen to allow for software calibration adjustments, so the span of the summing amplifier overlaps the possible full Span of 0 to 19.999999V at both extremes:

With an overall 25-bit count of zero in the comparators, REF+Ve is +3.2mV minus +23.5mV, a negative overlap of −20.3mV.

At overall full count, REF+Ve is +20.6V minus +20.9mV, approximately +20.58V.

4.6.10.4 Bipolar Reference Switching

Relays RI1 and RL2 are used in DC calibrators for polarity reversal. This is not necessary in the 4200, and during operation RL1 is always de-energized, while RL2 is energized. Thus all outputs from the summing buffers are fed to the AC Assembly via RL2.

4.6.11 Quasi-Sinewave Generation

4.6.11.1 Quasi-Sinewave Reference

In the Sense/Reference comparator, a considerable advantage is gained by comparing AC with AC. (If AC sense were compared with DC reference, small DC offsets would be magnified, leading to 'DC turnover' errors). The AC waveform used as reference is constructed in ten steps by a digitally controlled switching network, based on the DC reference as its peak value. It has been given the name 'Quasi-Sinewave'.

The comparator produces an error to drive the VCA, which is proportional to the difference in 'Mean Square' values, and is driven to zero by the action of the Output-Sense loop. At zero error the RMS value of the comparator's sense input has thus been adjusted by the loop to be equal to the RMS value of its reference input.

On the 1V Range there is neither amplification nor attenuation in the Output-Sense loop. The quasi-sinewave is designed so that with the 1V Range selected, its RMS value is equal to the voltage demanded on the front panel OUTPUT display, (with small, controlled adjustments for calibration).

On higher ranges, decades of amplification are switched in to set the output to the demanded voltage. Switched decades of attenuation reduce the sensed sinewave back to the 1V-Range level for comparison with the quasi-sinewave.

On millivolt ranges the 1V sense loop is used with precise, passive, decade attenuators reducing the output to the values on the display.

On current ranges, the current reference is derived from either the closed 1V or 10V Range Output/Sense loop.

Therefore on all ranges the Output/Sense loop gain is driven to a magnitude of 1, so that the VCA and the comparator both operate at 1V Range levels.

4.6.11.2 4200 DC Reference Scaling

The Reference Divider hardware is common to several instruments. In DC calibrators, the basic voltage range is usually the 10V Range, with 100% overrange at Full Scale. In these cases the full span of reference values is employed, generating the resolution necessary to accommodate the DC accuracy available.

The same accuracy is not available for AC, so the high resolution is not necessary. Moreover, the linearity of the analog circuitry is improved by using a smaller dynamic range in the reference circuits. So in the 4200 the 1V Range is the basic range, and the software scales its demanded value accordingly.

In the 4200 the sensed output is compared against the quasi-sinewave whose characteristics match those of the sensed sinewave. To construct the quasi-sinewave, the DC reference voltage needs to be set at its peak value.

The microprocessor program imposes, in software, the scaling factors which establish the reference voltage at the peak value of the quasi-sinewave. Thus the full span of the 25-bit comparator, and hence the possible dynamic range of the DC reference, are realized only at times when the Reference Divider itself is being calibrated. Before initial calibration, the maximum obtainable reference voltage is slightly greater than 2.8V, and the minimum is slightly less than 125mV. This overlaps the peak voltages of the quasi-sinewaves corresponding to the maximum and minimum values of sensed output; giving a margin for accurate calibration, from digital gain factors held in the non-volatile calibration memory.

4.6.11.3 DC Reference Voltage Values

As mentioned earlier, the DC Reference is used to establish the amplitude of the quasi-sinewave. When the 1V Range is selected, the reference is set to the peak value of the quasi-sinewave, which is 1.397 times the demanded RMS (sinewave) voltage output of the instrument. In normal use, therefore, the reference voltage is adjusted by front panel OUTPUT display selections; between 125.7mV (for 0.9V selection) and 2.79V (for 1.999999V selection), plus or minus any user-calibration corrections.

On higher and lower ranges, analog range switching in the sense amplifiers scales the sense voltages for comparison with the same voltage span of quasi-sinewaves.

4.6.11.4 Reference Inverter

(Circuit Diagram 430447 page 7.7-2)

The quasi-sinewave is derived by a specific form of D-A converter, selecting voltages from a divider network. Because negative values are required, the divider is strung between positive and negative reference voltages; the unity-gain Reference Inverter generates the negative reference 'REF-Ve' by inverting 'REF+Ve'.

M1, M2 and Q1 perform the inversion. M2 generates the bandwidth necessary for amplitude switching operations, while chopper-stabilized integrator M1 removes DC offsets, always referring the inverter output to Common-2C. To compensate for RMS value changes in the quasi-sinewave (due to switching errors arising from frequency changes), feedback from the quasi-sinewave is applied via R1, C4, R4 and C5. Q1 provides the output drive to the quasi-sinewave generator.

4.6.11.5 Quasi-Sinewave Generator

(Circuit Diagram 430447 page 7.7-3)

The SYNCØ input to M11 RESET is a decoded address which, when set to logic-1, disables the Quasi-sinewave sequence counter M11. It is permanently held at logic-Ø in the 4200, to enable the quasi-sinewave for both AC Voltage and Current functions.

The quasi-sinewave is generated at a frequency determined by the Frequency Synthesizer 100Hz-4kHz output (para 4.7.3.3 describes the synthesis), clocking the decade counter M11 via J7.50. This continuously recycles M11 in ascending count through $Q_Ø$ to Q_9, ten clocks constituting one cycle of the quasi-sinewave. So the quasi-sinewave runs at a frequency of between 10Hz and 400Hz, indeed the carry C_{out} of M11 returns to the Synthesizer via J7-51 to be selected as the reference frequency for the 100Hz (10-330Hz) frequency range.

With increase of frequency range, the difference between the frequencies of output and quasi-sinewave increases in decade steps. As the comparison of sense and quasi-sinewave signals is performed at mean-square DC levels, this difference theoretically does not matter, so long as the signal is at an exact multiple of the quasi-sinewave frequency. However, to achieve optimum operation of the Sense/Reference comparator, the zero crossings of the quasi-sinewave are synchronized to occur coincident with a sense signal zero crossing.

Synchronization is achieved by the clock input to M9, controlling the timing of the quasi-sinewave switches M8 and M14. Using the same clocks, M11 and M10 transit times prevent the data from arriving at M9 'D' inputs until the data already established there by the previous clock pulse has been latched at its outputs. Thus data ripples through M11 and M9 at successive clock pulses.

The ripple rotates the data by one clock period and would, if left uncorrected, put the switching out of sequence. The arrangement of the connections between M11 outputs and M9 data inputs, combines appropriate outputs so as to correct the switching pattern. The table in Fig. 4.6.11 demonstrates the rotation of 1 clock period; the quasi-sinewave steps being labelled at M9 inputs and outputs.

The quasi-sinewave is output to the transfer switching input to the Sig/Ref comparator at M16-1. The action of the transfer switch is described in section 4.14.

A second output is filtered and fed back as compensation to the Reference Inverter as described earlier (para 4.6.11.4).

Step	0	1	2	3	4	5	6	7	8	9
M11 Output at Logic-1:	Q_9	$Q_Ø$	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
M10 Output pin at Logic-1:	4	11	—	11	4	10	3	—	3	10
M9 Output pin at Logic-1:	O_1	O_4	O_5	O_4	O_1	O_2	$O_Ø$	O_3	$O_Ø$	O_2
Switch Energized M8 pin: / M14 pin:	5 / —	6 / —	13 / —	6 / —	5 / —	— / 5	— / 6	— / 13	— / 6	— / 5
Step Voltage Fed to M16-1:	+0.42	+1.16	+1.397	+1.16	+0.42	−0.42	−1.16	−1.397	−1.16	−0.42

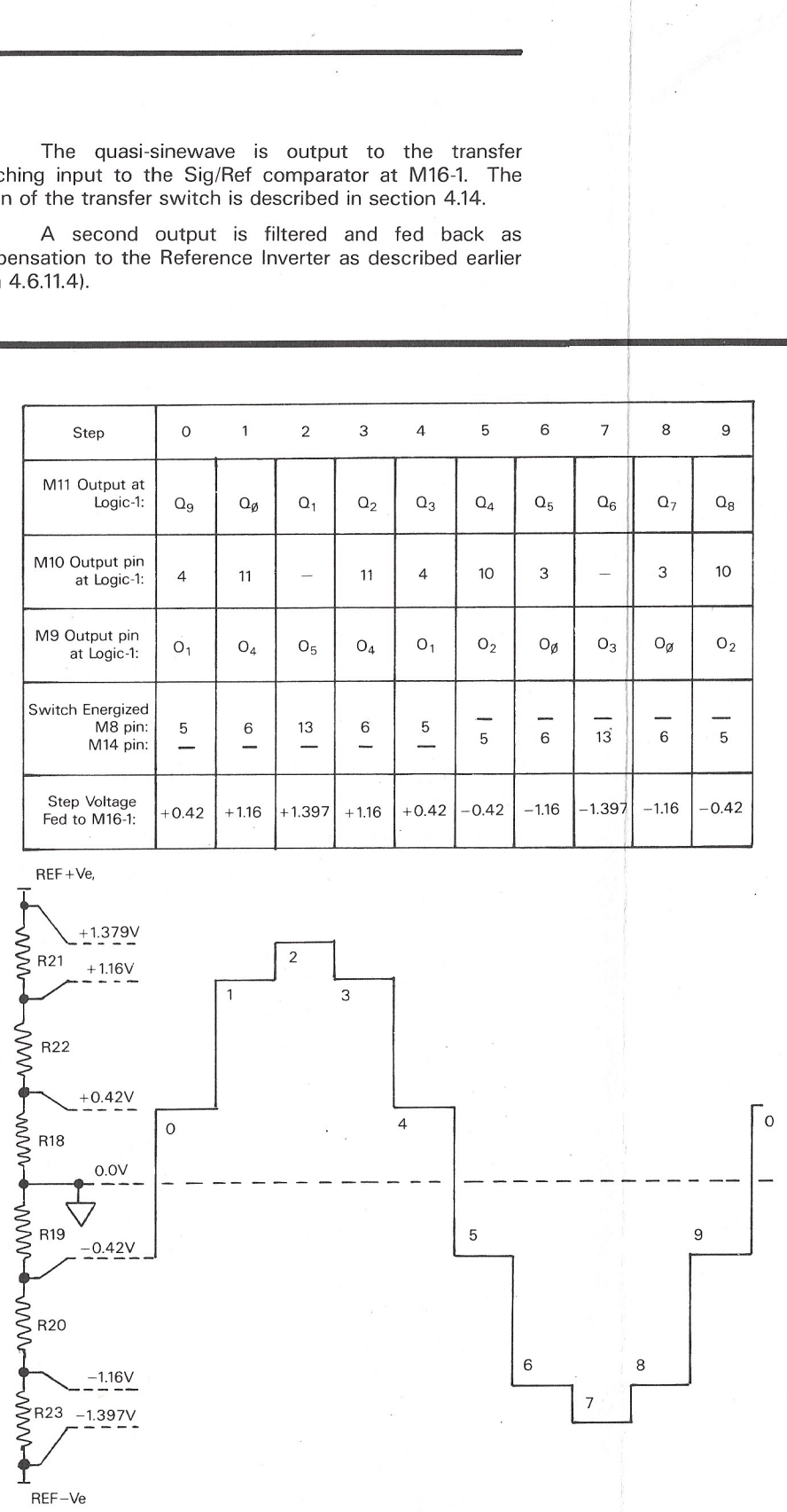


FIG. 4.6.11 QUASI-SINEWAVE GENERATION

4.7 DIGITAL FREQUENCY SYNTHESIZER
(Fig. 4.7.1)

4.7.1 General

Users normally set the 4200 operating frequency by a combination of 'FREQUENCY RANGE' and 'FREQUENCY' display selections. These are memorized by the CPU and translated into two binary control words:

'$FREQR_{2-\emptyset}$', a three-bit word, five of whose codes represent the five frequency ranges.

'$FREQ_{8-\emptyset}$', a nine-bit word whose value 'n' defines the chosen frequency with respect to the selected frequency range.

Users can select a frequency by means other than pressing a FREQUENCY RANGE key and setting a frequency on the display; for example by using 'Store', 'Spot F' or the IEEE488 digital interface. But regardless of the selection method, the CPU will always compute the two binary words, which then synthesize the selected frequency in the Sine-Source Assembly.

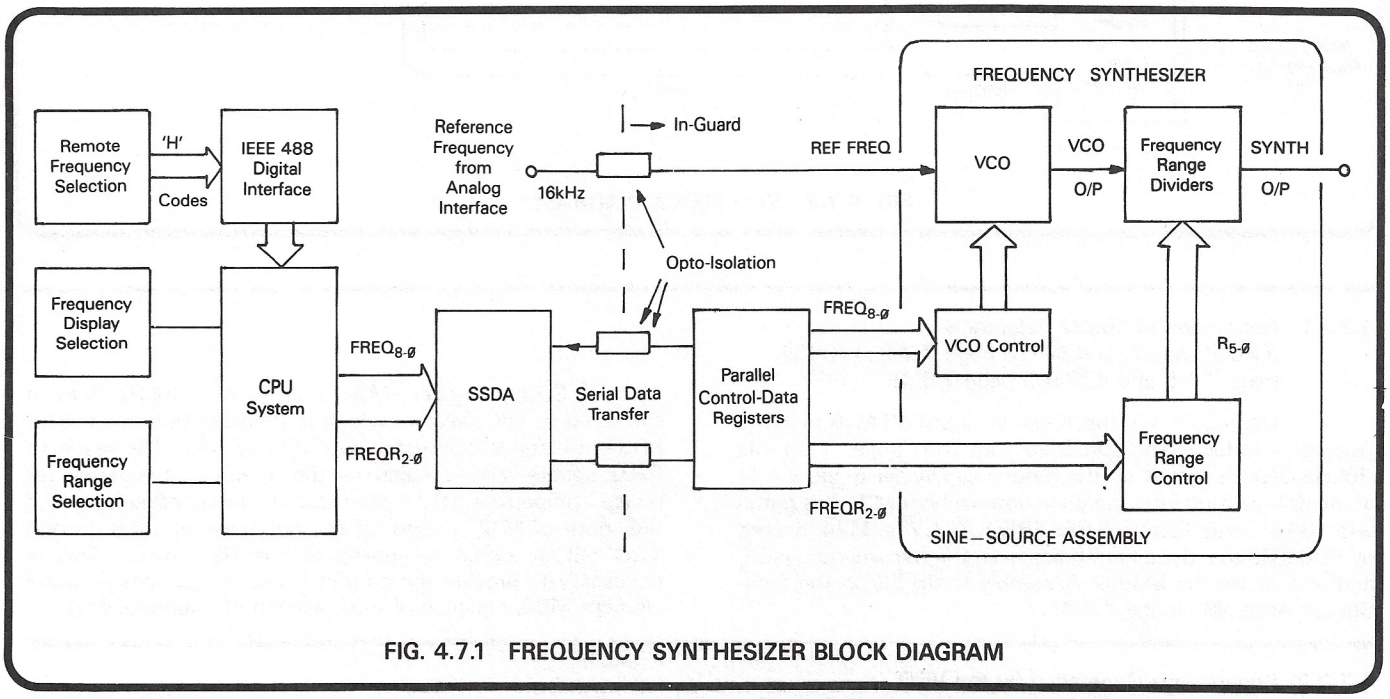


FIG. 4.7.1 FREQUENCY SYNTHESIZER BLOCK DIAGRAM

Both words are passed into guard via the SSDA, and latched at the outputs of the Reference Divider Parallel Control registers. A 16kHz reference frequency is also taken into guard, to be divided by two to 8kHz in the Sine-Source.

After entering the Sine-Source assembly, $FREQ_{8-\emptyset}$ effectively multiplies the 8kHz reference by 'n' to determine the frequency of a Voltage Controlled Oscillator (VCO). The VCO frequency (signal 'VCO O/P') is input into a series of frequency dividers, whose ratios are set by $FREQR_{2-\emptyset}$. The division ratios are chosen so as to make the dividers generate the Frequency Synthesizer output signal ('SYNTH O/P') at the user-selected frequency.

The purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The oscillator is approximately tuned by selection of circuit constants using '$FREQR_{2-\emptyset}$' and '$FREQ_{8-\emptyset}$'.

'SYNTH O/P' acts as the reference in the phase comparator of a Phase-Locked Loop, controlling the frequency of the main Quadrature Sinewave Oscillator to an accuracy determined by the crystal oscillator.

4.7.2 Voltage Controlled Oscillator

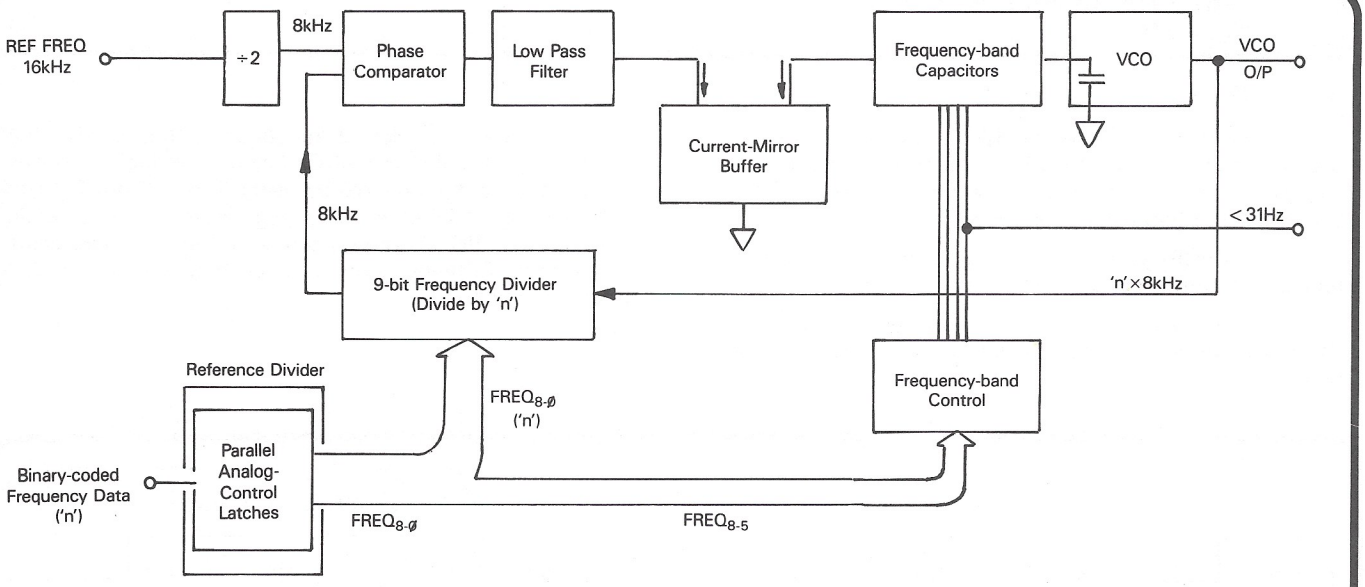


FIG. 4.7.2 VCO BLOCK DIAGRAM

4.7.2.1 Generation of 16kHz Reference

(Circuit Diagrams 430570 page 7.3-2, 430535 page 7.4-5 and 430446 page 7.6-4)

On page 7.3-2, the 16kHz is picked off M16-14 in the Analog Interface and buffered out on page 7.3-1 as '16kHz(OG). It arrives on the Reference Divider (page 7.4-5) at J4-104, passing into guard via opto-isolator M3. It is gated with 'BARK' and 'DISABLE REF FREQUENCY' in M24, filtered by R86/C38 to reduce harmonics from the transmission path, and is sent via the Mother Assembly to J6-53 on the Sine-Source Assembly (page 7.6-4).

Schmitt-trigger M14 inverts the 16kHz into a symmetrical squarewave, which is then applied as clock to M13a, a bistable connected to divide by two. The resulting 8kHz squarewave is taken as the reference frequency for phase comparator M12. Note that in this configuration the SIG input of M12 is used for the reference, and the divided VCO output signal is applied to the REF input. This is necessary to provide the correct sense in the phase control element M50, because of the inversion of integrator M11.

4.7.2.2 Squarewave Generation by the VCO

The VCO is a discrete-component ECL relaxation oscillator generating an output of frequency 'n' x 8kHz. Its natural frequency is dependent on:

a. the value of the timing capacitor C2 (or C2 plus one of C3-C6 in parallel),

b. the value of its continuous discharge current through the phase control element (current mirror M50), and

c. the value of its charging current through Q2 on alternate half cycles (4.7mA).

Consider C2 fully discharged. Q4 is off, so the 4.7mA from Q6 is all passing through Q5. The collector voltage of Q4 is close to the positive rail, and is emitter-followed to the base of Q5 via R9, holding Q5 on. Also, because Q3 is turned off by Q4 collector voltage, Q2 is turned on at its emitter, passing 4.7mA into C2 and the current mirror M50.

C2 charges until Q4 turns on at its base-emitter threshold. Cumulative Schmitt action passes the fall at Q4 collector to the base of Q5, ensuring a rapid transition between states so the 4.7mA is transferred from Q5 to Q4. Q3 turns on, its emitter falling quickly to cut Q2 off, so the charging path to C2 etc. is interrupted.

M50 continues to discharge C2, whose voltage falls slowly until Q4 starts to cut off again. The cumulative action is repeated to turn Q2 on, recharging C2. The cycle of charge and discharge continues, generating 'VCO O/P' squarewaves at buffer Q12 emitter.

4.7.2.3 Coarse Frequency Control

(Circuit Diagram 430446 Page 7.6-4, and Fig. 4.7.2)

At any time, only one of the capacitors C3, C4, C5 and C6 can be connected in parallel with C2, by conduction of its associated transistor. This splits the frequency range of the VCO into five bands, governed by the four most-significant bits of the frequency control word $FREQ_{8-\emptyset}$ acting on M8. The association is shown in Table 4.7.1, note that the VCO frequency bands quoted in the table are correct only because the VCO is under the fine control of comparator M12, within the phase-locked loop.

$FREQ_{8-5}$ bits 8 7 6 5	Range of 'n' Values	M8 Outputs at Logic-1	C2-C6 Selection	VCO Frequency Band (kHz)
0 0 0 0	10 to 31	$X_\emptyset$	C2 and C6	80 to 248
0 0 0 1	32 to 63	X_1	C2 and C5	256 to 504
0 0 1 X	64 to 127	X_{3-2}	C2 and C4	512 to 1016
0 1 X X	128 to 255	X_{7-4}	C2 and C3	1024 to 2040
1 X X X	256 to 500	NONE	C2 only	2048 to 4000

TABLE 4.7.1 COARSE FREQUENCY CONTROL

4.7.2.4 Fine Frequency Control

(Circuit Diagram 430446 Page 7.6-4, and Fig. 4.7.2)

In the following description, capacitors C3, C4, C5 and C6 are ignored, but references to C2 should be read as including the appropriate additional capacitor.

The VCO output is fed back to M12 phase comparator via M9 and M13b, which are connected to act as a 9-bit frequency divider. Because the divider is controlled by $FREQ_{8-\emptyset}$, the VCO output frequency is always divided by 'n' before being applied to the REF input of the comparator. The output from the comparator will only be zero if the frequency fed back to M12-6 is 8kHz (ie. the VCO frequency is n×8kHz), and in phase with the 8kHz REF FREQ at M12-3 (TP14).

The output from M12 is integrated by M11 to drive a DC current into the current mirror M50. The current mirror has a gain of two, its output current being drawn from the charge on C2. During the half-cycles of the VCO oscillation when C2 is being charged, the mirror obtains its current from Q2 conduction.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C16 and C18 have no charge or discharge path, so M11's extremely high gain maintains the charge on the capacitors, and the voltage at TP6. M11 supplies the input current for M50, the mirror continues to draw the same discharge current from C2, so the frequency of VCO oscillation remains constant. Thus the loop stabilizes only when the frequency divided by 'n' from the VCO output is in phase with (and therefore at the same frequency as) the reference 8kHz.

In stable operation, therefore, the loop maintains VCO oscillation at n×8kHz, and the feedback dividers reduce this frequency by a factor of 'n' to 8kHz.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M12. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

4.7.2.5 'INHIBIT' (VCO Off)

The VCO can be switched off by a logic-1 of OV at the base of Q11 (INHIBIT signal). This originates in the CPU system, setting $FREQR_{2-\emptyset}$ code to 111 (a non-existent 'R7' range). This INHIBIT signal is not used in the 4200.

4.7.2.6 VCO Supply Rail Protection

To prevent VCO oscillations appearing on the ± 15V power rails, which also supply the integrator M11 and current mirror M50, the positive rail is heavily decoupled, regulated by Q8, and all devices whose currents are likely to disturb the rails are supplied through constant current sources (Q1, Q6, Q9 and Q13).

4.7.2.7 VCO Output

The VCO, integrator and current mirror operate from the ± 15V supplies. The phase comparator, divide-by-'n' counter and the frequency dividers which follow the VCO, all operate from the in-guard logic supplies of 0V and −15V. The VCO output from Q12 emitter is therefore limited by D1 to logic supply levels. A conversion from logic supply levels back to ± 15V levels is accomplished at the input to the integrator M11, as TP31 pulses are negative at M11 input.

D1 is a Schottky hot carrier diode of reverse capacitance approx. 2pF to avoid distorting the high frequency squarewaves it is limiting (for 1MHz 4200 output, the VCO oscillates at 4MHz).

The output is passed through R12 to avoid loading the VCO, and then fed as 'VCO O/P' to the frequency dividers at M5-9 (page 7.6-5)

4.7.3 Frequency Range Dividers
(Fig. 4.7.3)

As mentioned earlier in para 4.7.1, the purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The VCO frequency (signal 'VCO O/P') is input to a series of frequency dividers, whose ratios are set by '$FREQR_{2\text{-}\emptyset}$', so as to make the dividers generate the selected frequency as 'SYNTH O/P'. $FREQR_{2\text{-}\emptyset}$ is a three-bit word, five of whose codes represent the five frequency ranges.

A second purpose is to clock the Quasi-Sinewave Generator in synchronism with the synthesizer output (and hence with the main quadrature sinewave oscillator output). The synthesizer frequency is a multiple of the Quasi-Sine frequency, except on the 100Hz frequency range, where they are both at the same frequency. Thus the divider ratios are also chosen to generate the correct frequencies for the quasi-sinewave clock, for each frequency range selected.

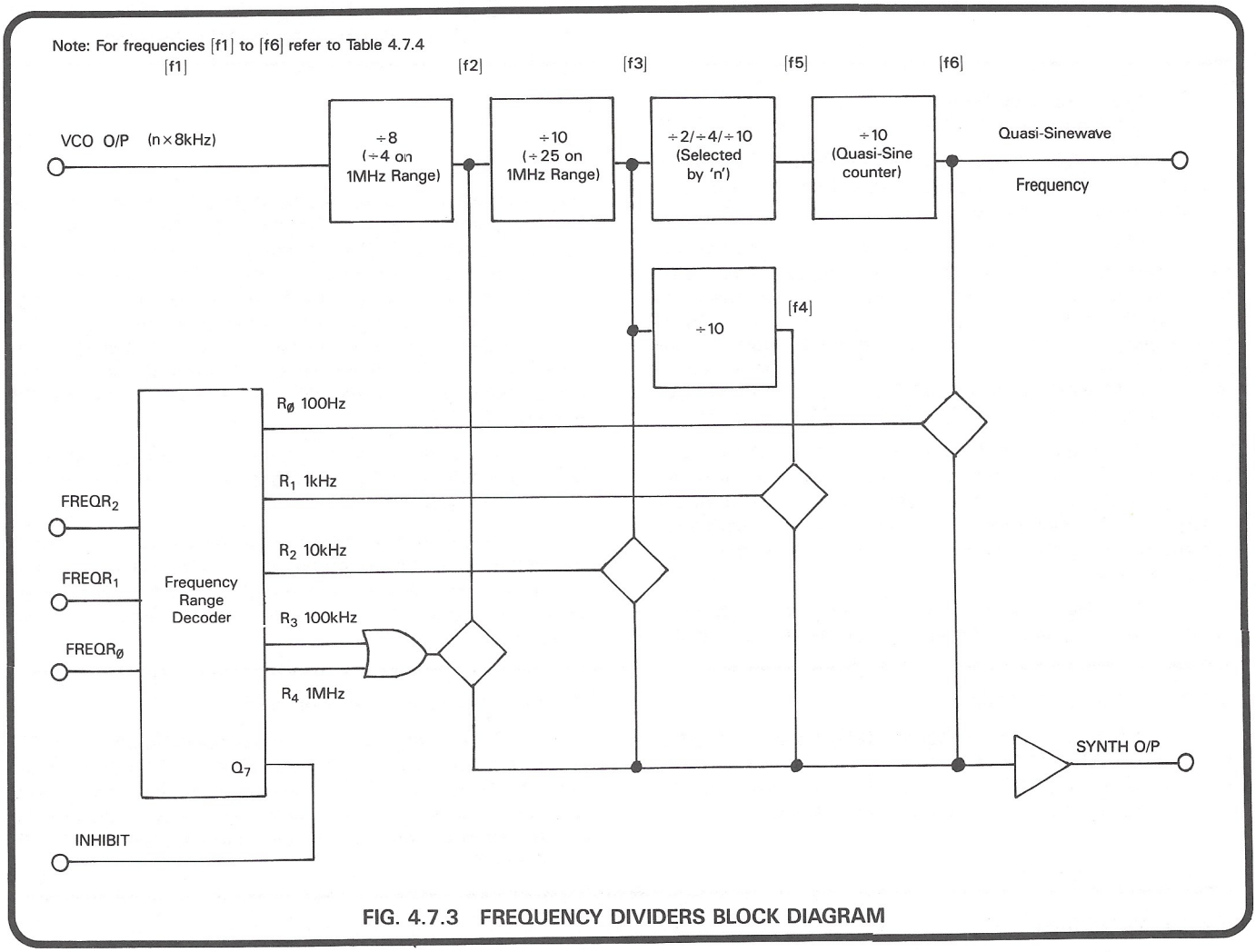


FIG. 4.7.3 FREQUENCY DIVIDERS BLOCK DIAGRAM

4.7.3.1 Divider Ratios
(Circuit Diagram 430446 Page 7.6-5)

Binary/BCD Divider M5 is set for binary division by M5-2 and M5-10 set to Logic-Ø. Conversely, M1 is set for decimal division by M1-2 and M1-10 at Logic-1.

BCD counter M2 is set to count up, by M2-10 at Logic-1. Its $\overline{\text{CARRY OUT}}$ signal at M2-7 is at one tenth of its clock frequency, and its Q1 output on M2-6 is at half its clock frequency. Flip-flop M4 is connected to divide its clocks by two.

Multiplexer M6 selects the appropriate source frequency to clock the Quasi-Sinewave generator. In particular, on the 100Hz Range it selects the $\overline{\text{CARRY OUT}}$ from M2, which is divided by 10 in the quasi-sinewave counter, and returned via J6-51 to be used as SYNTH O/P.

4.7.3.2 Ratio Selection by Frequency Range
(Fig. 4.7.3 and Table 4.7.2)

The frequency range selection word $FREQR_{2-Ø}$ is decoded by M29 into five range lines $R_{4-Ø}$. These lines perform the following functions:

a. They switch ranges in the quadrature sinewave oscillator by relay RL1-RL8 selection of integrator capacitors (page 7.6-1);

b. They switch ranges in the Cosine Squarer output filter (page 7.6-2);

c. They adjust the division ratios of Frequency Range Dividers M5 and M1 (page 7.6-5) for range R4 (1MHz Range); and

d. They select appropriate outputs from the Frequency Range Dividers (page 7.6-5).

Functions (a) and (b) are described later in Section 4.8. In this description we are concerned only with functions (c) and (d).

Table 4.7.2 shows how frequency range switching derives the synthesizer output frequencies by selecting the appropriate outputs from the dividers. Note that except for the 1MHz Range R4, the ratios of individual dividers are not altered.

On the 100Hz Range RØ the overall division ratio of 8000 is achieved as for the 1kHz Range, but with a further division by 10 in the quasi-sinewave counter M11 on the AC Assembly.

On the 1MHz Range R4, the division ratio of M5 is changed from 8 to 4. The DP_A inputs M5-5 and M5-6 are primed to Logic-1 and Logic-Ø respectively, whereas on all other ranges the priming is reversed. Range R4 also alters the division ratio of M1 from 10 to 25, by changing its priming bit-pattern, to correct the quasi-sinewave frequency; but as the synthesizer output is taken through M10-4/3 from M5 output, the adjustment to M1 does not affect the SYNTH O/P frequency.

FREQ. RANGE	FREQUENCY DISPLAY	VCO OUTPUT (n×8kHz)	OVERALL DIVISION RATIO	RELEVANT DIVIDER RATIOS				QUASI-SINE CLOCK FREQUENCIES	SYNTHESIZER OUTPUT
				M5	M1	M2	M11* (AC PCB)		
	Hz	kHz						(J6-50)*	(J6-52)
100Hz (RO)	10-63 64-127 128-330	80-504 512-1016 1024-2640	8000	8 8 8	10 10 10	10 10 10	10 10 10	Hz 100-630 640-1270 1280-3300	Hz 10-63 64-127 128-330
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	240-504 512-1016 1024-2640	800	8 8 8	10 10 10	10 10 10		kHz 1.5-3.15 1.6-3.175 1.28-3.3	Hz 300-630 640-1270 1280-3300
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	240-504 512-1016 1024-2640	80	8 8 8	10 10 10			kHz 1.5-3.15 1.6-3.175 1.28-3.3	kHz 3.0-6.3 6.4-12.7 12.8-33.0
100kHz (R3)	30k-63k 64k-127k 128k-330k	240-504 512-1016 1024-2640	8	8 8 8				kHz 1.5-3.15 1.6-3.175 1.28-3.3	kHz 30-63 64-127 128-330
1MHz (R4)	0.30M-1.00M	1200-4000	4	4				kHz 1.2-4.0	kHz 300-1000

* Quasi-sine counter M11 on the AC Assembly divides VCO output at all frequencies, but contributes to SYNTH O/P only on the 100Hz Frequency Range.

TABLE 4.7.2 SYNTHESIZER OUTPUT—DIVISION RATIOS

4.7.3.3 Frequency Synthesis for the Quasi-Sinewave Generator
(Fig. 4.7.3 and Table 4.7.3)

The 100Hz frequency range uses the quasi-sinewave counter as a divider in deriving its SYNTH O/P frequency. Although not directly related to the frequency of the SYNTH O/P signal on other ranges, the quasi-sinewave frequency is deliberately derived in the synthesizer, so that the zero-crossings of its waveform can be synchronized at a time when the main sinewave is also crossing zero. (The main sinewave, of course, can be at a high multiple of the quasi-sinewave frequency.)

The quasi-sinewave frequency is held to a maximum of 330Hz (400Hz on the 1MHz range), to limit errors due to high harmonics. The 1MHz frequency range contains only one frequency band, but the other four ranges are each divided into three bands, corresponding to the three most significant bits of the frequency word $FREQ_{8\text{-}Ø}$.

Table 4.7.3 illustrates the way that the three bands affect the quasi-sine frequencies. Note that division ratios of 2, 4 or 10, by M2 and M4a, are selected by $FREQ_6$, $FREQ_7$, and $FREQ_8$ at M6 pins 11, 10 and 9 respectively. Frequency range RØ at M7-2 ensures that on the 100Hz range, the divide-by-10 output of M2 is always selected, regardless of the state of these three bits.

To ensure that the Divide-by-2 outputs of M2 and M4a are locked into the correct phase for quasi-sinewave generation, a 'CHOP LOCK' synchronizing signal is derived from the quasi-sinewave counter 'Q_0' output, entering at J6-75. Following DC-restoration from ±8V supplies to the normal 0V/−15V logic supplies by C20/D3/R15/M7, the signal is applied to M4a SET input, and M2 RESET input.

For all 4200 frequency ranges, the '100-5kHz' quasi-sinewave generator clock is passed to the AC Assembly via J6-50 and the Mother Assembly. This output is level-shifted by Q42, to the ±8V supplies which are used in the quasi-sinewave generator circuitry. Quasi-sinewave synchronizing signal 'SYNC Ø (IG)' (which was transferred into Guard by M2 on the Reference Divider), is input to the Sine-Source Assembly on J6-48 to be similarly level-shifted by M43, before being passed to the AC Assembly via J6-49.

For other details of the quasi-sinewave generator refer to para 4.6.11.

FREQ. RANGE	FREQUENCY DISPLAY Hz	FREQUENCIES SYNTHESIZED IN SINE-SOURCE ASSEMBLY				QUASI-SINE FREQUENCY (& J7-51) Hz	4200 OUTPUT FREQUENCY Hz
		VCO OUTPUT (n×8kHz) kHz	DIVIDER RATIOS for QUASI-SINEWAVE M5 M1 M2 M4a	OVERALL DIVISION RATIO	QUASI-SINE CLOCK FREQUENCY (J7-50)		
100Hz (RØ)	10-63 64-127 128-330	80-504 512-1016 1024-2640	8 10 10 — 8 10 10 — 8 10 10 —	800 800 800	Hz 100-630 640-1270 1280-3300	10-63 64-127 128-330	10-63 64-127 128-330
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	240-504 512-1016 1024-2640	8 10 2 — 8 10 2 2 8 10 10 —	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	240-504 512-1016 1024-2640	8 10 2 — 8 10 2 2 8 10 10 —	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k
100kHz (R3)	30k-63k 64k-127k 128k-330k	240-504 512-1016 1024-2640	8 10 2 — 8 10 2 2 8 10 — —	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	30k-63k 64k-127k 128k-330k
1MHz (R4)	0.30M-1.00M	1200-4000	4 25 10 —	1000	kHz 1.2-4.0	120-400	0.30M-1.00M

TABLE 4.7.3 QUASI-SINEWAVE FREQUENCY DERIVATION IN FREQUENCY SYNTHESIZER

4.7.3.4 Synthesizer Frequency Analysis

Table 4.7.4 is provided to allow a complete analysis of the frequencies to be found in the divider circuitry. In part, it duplicates figures from tables 4.7.2 and 4.7.3.

FREQ. RANGE (NOM)	FREQUENCY DISPLAY Hz	VCO DIVISOR 'n'	f1 VCO OUTPUT (n × 8kHz) kHz	f2 M5 OUTPUT (f1 ÷ 8) kHz	f3 M1 OUTPUT (f2 ÷ 10) kHz	f4 M2 OUTPUT (f3 ÷ 10) Hz	f5* M6 OUTPUT (M6-3) Hz			f6 J6-51 INPUT (f5 ÷ 10) Hz
							M6 Input Channels and Division Ratios			
							$X_{\emptyset}$ (f3 ÷ 2)	X_1 (f3 ÷ 4)	$X_{2\text{-}7}$ (f3 ÷ 10)	
100Hz (RØ)	10-63 64-127 128-330	10-63 64-127 128-330	80-504 512-1016 1024-2640	10-63 64-127 128-330	1.0-6.3 6.4-12.7 12.8-33.0	100-630 640-1270 1280-3300			100-630 640-1270 1280-3300	[10-63] [64-127] [128-330]
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	30-63 64-127 128-330	240-504 512-1016 1024-2640	30-63 64-127 128-330	3.0-6.3 6.4-12.7 12.8-33.0	[100-630] [640-1270] [1280-3300]	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	30-63 64-127 128-330	240-504 512-1016 1024-2640	30-63 64-127 128-330	[3.0-6.3] [6.4-12.7] [12.8-33.0]	100-630 640-1270 1280-3300	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
100kHz (R3)	30k-63k 64k-127k 128k-330k	30-63 64-127 128-330	240-504 512-1016 1024-2640	[30-63] [64-127] [128-330]	3.0-6.3 6.4-12.7 12.8-33.0	100-630 640-1270 1280-3300	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
1MHz (R4)	Hz 0.30M-1.00M	'n' 150-500	kHz 1200-4000	(f1 ÷ 4) kHz [300-1000]	(f2 ÷ 25) kHz 12-40	(f3 ÷ 10) Hz 1200-4000			1200-4000	Hz 120-400

Note:
Frequency spans in square brackets [. .] are the SYNTH O/P frequencies on those ranges.
Other frequencies are present and may be tested.

*Quasi-sine counter M11 on the AC Assembly divides VCO output at all frequencies, but contributes to SYNTH O/P only on the 100Hz Frequency Range.

TABLE 4.7.4 SYNTHESIZER DIVIDERS—FREQUENCY ANALYSIS

4.8 QUADRATURE SINEWAVE OSCILLATOR
(FIG. 4.8.1)

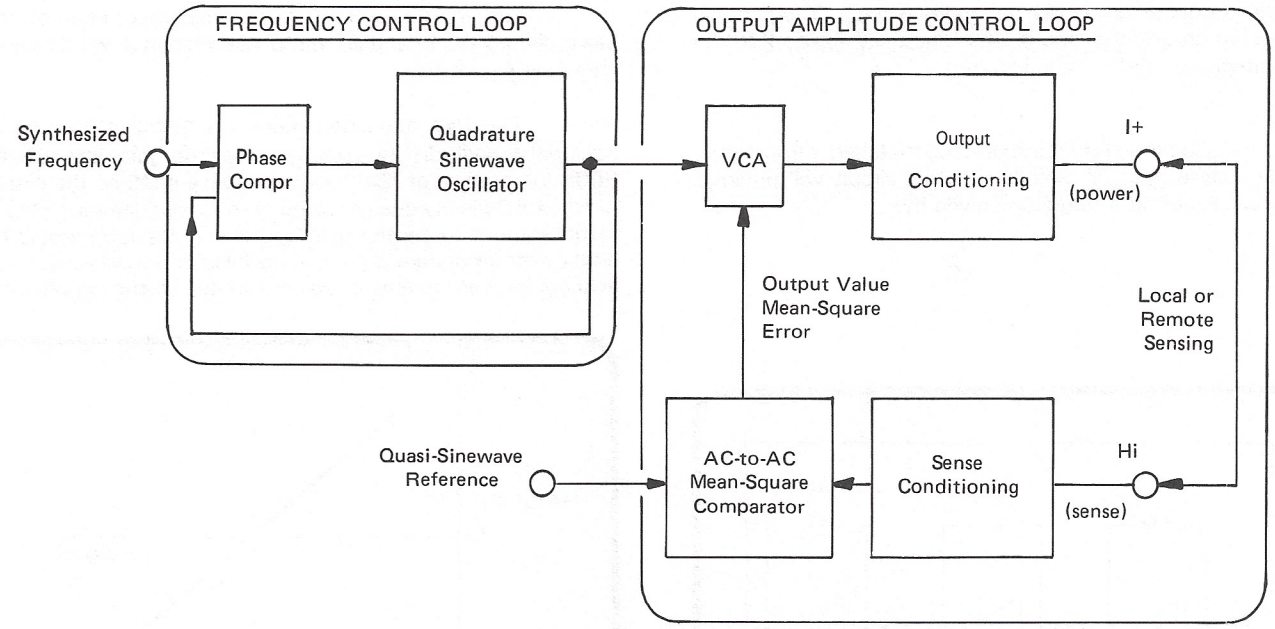


FIG. 4.8.1 THE QUADRATURE SINEWAVE OSCILLATOR AND ITS SYSTEM ENVIRONMENT

4.8.1 Purpose and Environment

The purpose of the oscillator is to define the amplitude-stability, purity and frequency of the sinusoidal output of the instrument on all ranges. Its output is of sufficient constant amplitude to drive the subsequent signal-conditioning circuitry.

After originating in the oscillator, the sinewave amplitude is accurately defined in two output-sense loops, using a low-distortion VCA as control element. The sinewave is set close to its demanded value by analog conditioning in the output circuits.

The output voltage is sensed, attenuated to its 1V Range equivalent, then its mean-square value is compared against that of the quasi-sinewave reference. The difference is converted into a DC error voltage which corrects the output by adjusting the VCA gain.

As the purity and amplitude-stability of the output sinewave depend substantially upon its source, a high quality oscillator is necessary. A 'quadrature' (dual-integrator) circuit is chosen for two main reasons:

a. This arrangement allows extensive phase and amplitude controls to be applied, to establish the required high specification.

b. Its natural frequency can be easily programmed by electrical selection of its component values.

The oscillator is approximately tuned by selection of circuit constants using the two CPU-derived binary words '$FREQR_{2\text{-}\emptyset}$' and '$FREQ_{8\text{-}\emptyset}$'. These also accurately define the crystal-sourced frequency of the Digital Frequency Synthesizer output, to which the oscillator is phase-locked. Thus the output sinewave frequency accuracy is held to 100ppm.

4.8.2 Simple Quadrature Oscillator
(Fig. 4.8.2)

4.8.2.1 Basic Circuit

The circuit consists of two RC integrators and an inverter, connected in a positive feedback loop. The nominal phase-shift around the loop is 360° (actually 720°: 270° in each integrator, 180° in the inverter).

Assuming perfect integrators, matched components and an inverter gain of exactly −1, this circuit will undergo stable oscillation at a frequency given by:

$$\omega_o = \frac{1}{R.C}$$

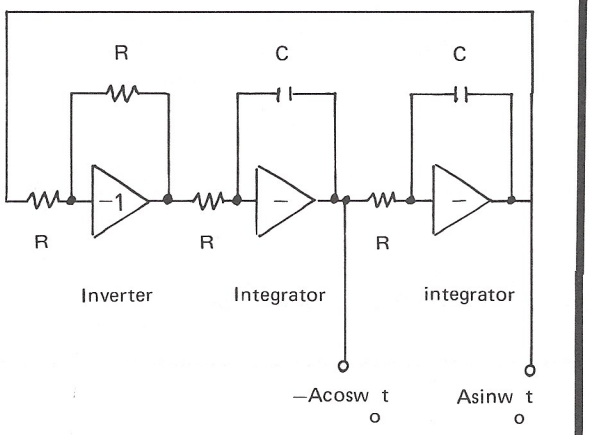


FIG. 4.8.2 BASIC QUADRATURE OSCILLATOR

4.8.2.2 Inadequacies of the Basic Circuit
(Fig. 4.8.2)

For an unrefined practical implementation of the basic circuit, the loop gain and phase response would be as shown in Fig. 4.8.3.

The two main conditions for stable oscillation at constant amplitude are: exactly unity loop gain, and exactly 360° (or multiple of 360°) of loop phase-shift; so the circuit of Fig. 4.8.2 clearly does not satisfy these conditions. Without some attempt to control gain and phase, the loop would be either over- or under-damped, so oscillations would either die away or increase in amplitude until limited by the supply rails.

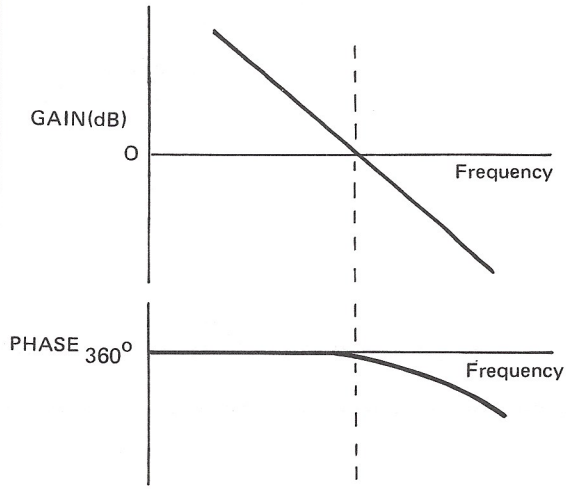


FIG. 4.8.3 GAIN AND PHASE RESPONSE OF PRACTICAL CIRCUIT

4.8.3 Practical Quadrature Oscillator
(Fig. 4.8.4)

The method chosen to refine the simple circuit corrects the loop phase-shift to exactly 360° using a feedback signal. Furthermore, it is arranged that this signal is correct only at a given output amplitude, so the amplitude of stable oscillation is defined. In Fig. 4.8.4 the correction circuit is added.

4.8.3.1 Phase Correction

The loop phase is corrected by introducing a small cosine term (B.cosωt) to be summed with the sine feedback (A.sinωt) at the input to the inverter. The resultant output of the inverter is thus given by:

$$V(t) = -(A.\sin\omega t + B.\cos\omega t) = M.\sin(\omega t + \phi) \qquad \text{——— 1}$$

where $M = \sqrt{A^2 + B^2}$

$\sin\phi = \frac{B}{M}$, and $\cos\phi = \frac{A}{M}$.

Hence $\phi = \tan^{-1}\frac{B}{A}$

and for B << A: $\phi \approx \frac{B}{A}$ ——— 2

The ϕ term represents an additional phase shift in the inverter, which by suitable scaling can be made equal to the phase error in the basis oscillator loop. Scaling is achieved by multiplying A.cosωt by the DC amplitude error ($A^2 - I_{REF}$), as described below.

4.8.3.2 Constant Amplitude Control

The above method of phase correction plays its part in controlling the output amplitude. With both sine and cosine terms available, a DC analog of the sinusoidal output amplitude can be obtained utilizing the identity:

$$\sin^2\omega t + \cos^2\omega t = 1.$$

Equal-amplitude sine and cosine outputs are squared in 4-quadrant multipliers. Their squares are summed to generate amplitude feedback in the form:

$$A^2.\sin^2\omega t + A^2.\cos^2\omega t$$
$$= A^2(\sin^2\omega t + \cos^2\omega t)$$
$$= A^2.$$

This method therefore expresses the square of the output amplitude as a DC current analog, from which is subtracted a constant DC reference current 'I_{REF}'. The difference current '$A^2 - I_{REF}$' is taken as the amplitude error, which defines the fraction 'B' of the cosine term to be fed back to the inverter as 'B.cosωt'.

In a perfect oscillator, this 'cos' feedback would be driven to zero. But in any practical circuit, some small remnant of B.cosωt persists at the correct loop phase-shift, correcting the loop gain to within the stability specification.

Acting thus together, the combined feedbacks correct both loop gain and phase simultaneously. The method of amplitude correction prevents the appearance of AC components in the amplitude error signal, thus avoiding unacceptable levels of harmonic distortion due to the cosine multiplier.

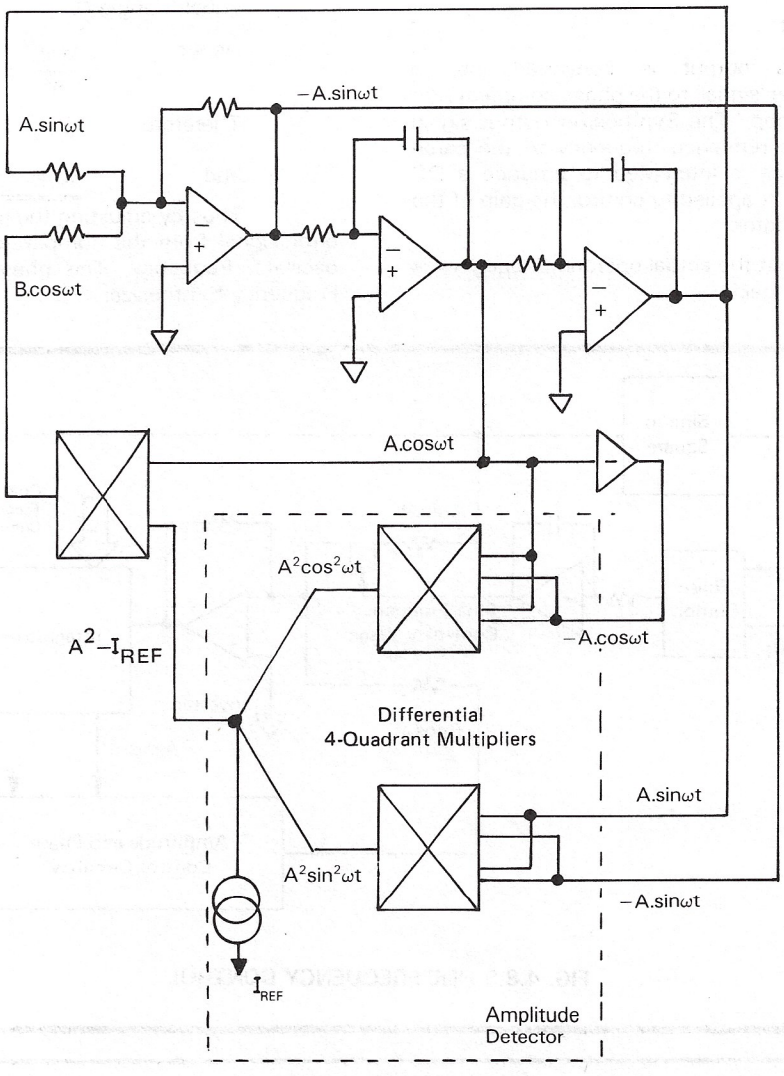


FIG. 4.8.4 CORRECTED QUADRATURE OSCILLATOR

4.8.4 Frequency Control
(Fig. 4.8.5)

Section 4.7 describes frequency generation in the Frequency Synthesizer. Binary control words computed by the CPU represent user-selections of FREQUENCY RANGE and FREQUENCY. These adjust frequency division ratios in the feedback circuit of a phase-locked loop, and division ratios in subsequent frequency dividers, to set the Synthesizer output signal 'SYNTH O/P' to the selected frequency. Stability and accuracy are assured by a crystal-sourced reference of 16kHz.

4.8.4.1 Coarse Adjustment

The Sinewave Oscillator is already approximately tuned to the selected frequency by the two binary control words, which select from weighted values of integration capacitance and resistance:

a. Frequency ranges are selected by the control word $FREQR_{2-\emptyset}$, which controls relays to change the values of integrator capacitance.

b. Frequencies within a range are selected by the control word $FREQ_{8-\emptyset}$, which controls FETs to change the values of integrator resistance.

4.8.4.2 Fine Adjustment

The oscillator's output is converted into a squarewave and applied as 'signal' to the phase comparator of a second phase-locked loop. The Synthesizer output signal 'SYNTH O/P' is input as reference frequency to the same comparator. The difference is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator.

It can be seen that the actual operating frequency is a function of the inverter gain:

In the frequency domain, the oscillator loop transfer function is given by:

$$G.\frac{\omega_o}{s} \cdot \frac{\omega_o}{s}$$

where G is the inverter gain,
ω_o is the unity-gain frequency
$s = j.\omega$, where ω is the actual frequency of operation.

For stable oscillation, the loop transfer function must equal 1 angle 0.

Hence $\frac{G.\omega_o^2}{s^2} = 1\underline{/0}$

Therefore $G.\omega_o^2 = j^2.\omega^2 = -1.\omega^2$

and $w = -\omega_o.G^{1/2}$

Thus by adjusting the gain of the inverter, the phase error signal from the comparator exerts fine control of the oscillator frequency. This phase-locks the oscillator to the Frequency Synthesizer.

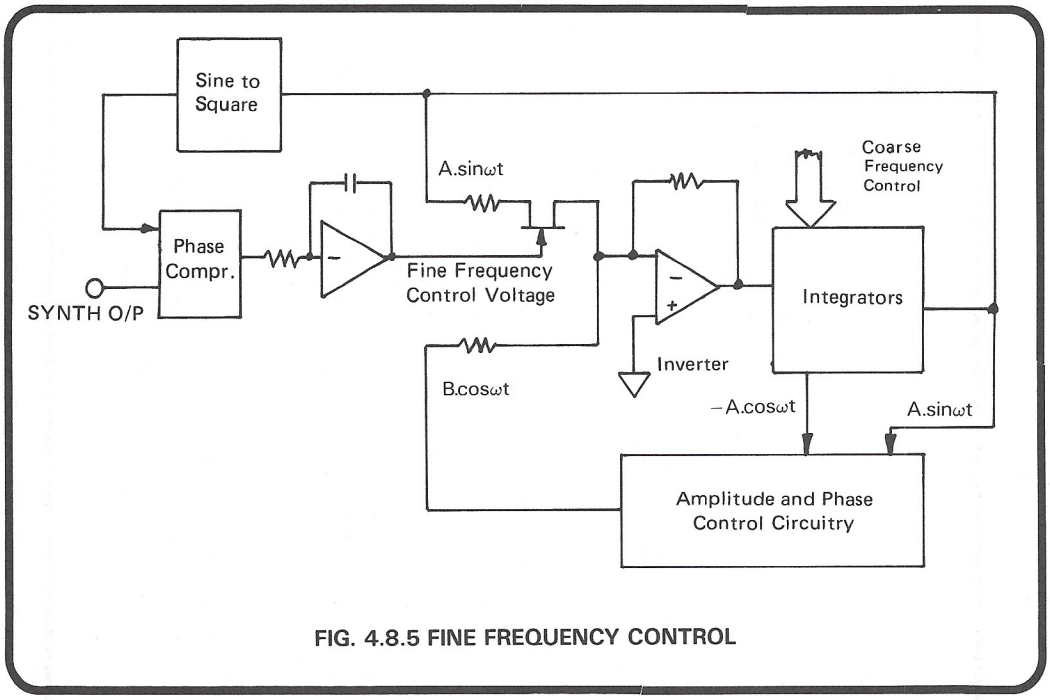


FIG. 4.8.5 FINE FREQUENCY CONTROL

4.8.5 Oscillator Output

The A.sinωt signal is inverted and buffered out to provide the drive to the output loop VCA. The buffer feedback resistors are positive TC thermistors which compensate for the TC of the VCA input FETs (refer to section 4.9).

4.8.6 Main Integrators

(Circuit Diagram 430446 page 7.6-1)

The cascaded integrators consist of M19 and M30 together with their input resistors and feedback capacitors. Both circuits are identical in operation, although some slight differences in implementation exist. Adjustments to the natural oscillation frequency are made by switching the integrator time constants.

4.8.6.1 Frequency Range Switching

The feedback capacitors are selected by the binary control word 'FREQ$R_{2\text{-}\emptyset}$'. This is decoded into five lines $R_{4\text{-}\emptyset}$ (page 7.6-5), each representing a frequency range. The capacitors for R_4 (1MHz) are fixed, one other set being added in parallel when its range is selected. Relays RL1 to RL8 perform the switching.

4.8.6.2 Frequency Increments

The integrator input resistors are connected in a binarily-weighted ladder network, the total input resistance depending on the pattern of FET conduction. Each FET is turned on by its corresponding binary digit in the frequency control word $FREQ_{8\text{-}\emptyset}$ (appearing as $A_{8\text{-}\emptyset}$ and $B_{8\text{-}\emptyset}$ at the FET gates).

The least-significant bits, representing low frequencies, control the highest-value resistors at the base of the ladder. The most-significant bits, which represent the highest frequencies, control the lowest-value resistors at the top.

Any user-selected frequency in a given frequency range is thus represented by a bit-pattern in the control word, which is repeated in the FET conduction pattern and resistance selection at the input of both integrators.

4.8.6.3 Slew Rate and Protection

Emitter-followers at the outputs of the integrator operational amplifiers allow the high slew-rates necessary to be achieved, by buffering loading effects. The diode clamp networks between output and input prevent latch-up by imposing unity-gain feedback when output peaks exceed approx. 5V.

4.8.6.4 Output Offset Control

The amplitude detector circuit squares the outputs from both integrators. It is therefore important that their DC offset voltages are not included in the squaring computation.

The 'Cosine' offset is removed by adjustment of R50 at the non-inverting input of M30, and the 'Sine' offset by R49 at the input of inverter M15. This latter adjustment removes the combined offsets of M15 and M19. (At manufacture, and after any replacement of major board components, the controls are iteratively adjusted for minimum AC fundamental component in the DC amplitude control signal 'V_G' at link 'B'.)

4.8.7 Inverter Stage

The inverter completes the positive feedback loop of the basic oscillator. The very high bandwidth device used for M15 is compensated by C27, and its TO8 case is grounded.

As mentioned earlier, its DC input offset is adjusted by R49 to null the sine DC offset.

4.8.7.1 Gain Control

The inverter has three inputs:

a. A.sinωt from the second integrator, the basic oscillator feedback loop.

b. B.cosωt from the Amplitude correction loop.

c. 'FREQ ERROR', a DC current which alters the inverter's input resistance (and hence its gain) by controlling FET conduction, phase-locking the oscillator to the synthesizer output frequency (refer to para 4.8.4.2).

Inputs a and b (A.sinωt and B.cosωt) are summed as currents at the inverting input. The amplitude of the B.cosωt signal is determined by the action of the amplitude control loop, described in sections 4.8.8 and 4.8.9.

Input c controls the gain of the inverter. The A.sinωt is applied via two input resistors R28 and R41 in series. R28 is shunted by the two FETs of Q29, whose the source-drain resistance is altered by the 'FREQ ERROR' current via current-mirrors M16 and M18.

Two FETs in series are required for the amplitude levels reached by A.sinωt. R41 is selected to account for differing 'on' resistances of different batches of FETs. This input circuit is a scaled-down version of that employed for the VCA in the main output loop, details of which appear in section 4.9.

A description of the action of the frequency tracking loop follows at para 4.8.7.2.

4.8.7.2 Frequency Tracking—General

As described in para 4.8.4.2, the oscillator's output is applied to the comparator of a phase-locked loop. The Synthesizer output is input as reference frequency to the same comparator. The phase-difference pulse train from the comparator is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator. This exerts fine control of the oscillator frequency, tracking the Synthesizer frequency.

4.8.7.3 Tracking Comparator
(Circuit Diagram 430447 Page 7.7-6)

After buffering and invertion by M47 on the Sine-source Assembly (page 7.6-1), the oscillator A.sinωt output is passed to the AC Assembly via J6-45 and J7-45.

On the AC Assembly, the sinewave is converted into a squarewave by Schmitt bistable Q23/Q33, and level-shifted to logic supply levels of 0V and −15V by D25/Q28. Q28 provides a current-limited load for maximum gain, while D24 and D25 prevent voltage saturation of Q32. Q23 buffers the resulting squarewave into the phase comparator input at M30-6.

The slower zero-crossings at the lowest frequencies could be susceptible to HF noise, so this is filtered, on the 100Hz frequency range only, by Q27 and C48.

The 'SYNTH O/P' squarewave, at the demanded frequency, is transmitted from the Sine-source Assembly at low (1V Full Range) level. This holds the maximum slew rate to a value which avoids inducing interference in other internal circuits. Q20 and Q21 amplify the signal to the CMOS logic levels of 0V and −15V required by the comparator input at M30-3.

Note that current steering is used between Q32 and Q33, and between Q20 and Q21. Also, a constant current source Q22 provides Q23 emitter current. These measures prevent the fast switching edges in the schmitt and amplifier circuits from injecting spikes into the supply rails.

Phase-comparator output M30-5 consists of positive pulses (0V) when the oscillator lags the synthesizer, or negative (−15V) when the oscillator leads. When both are in phase, M30-5 is at high impedance.

At integrator M31 input, zener diode D30 holds the non-inverting input at −6.4V; so for in-phase signals into the comparator, the inverting input seeks the same level. The integrator tends to hold its voltage level (with very slight drift due to capacitor leakage but limited to −9.8V by D32/D33). When the oscillator output lags the synthesizer output, the positive-going comparator pulses are integrated to drive M31-6 slowly more negative. When the phase of the oscillator leads, the integrator output becomes more positive.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C53 and C56 have no charge or discharge path, so M31's extremely high gain maintains a constant charge on the capacitors. The constant voltage on Q37 base maintains a constant 'FREQ ERROR' current.

Q37 appears to be an open-collector amplifier. However, its collector current passes via J7-44 and J6-44, into the two current-mirrors at the input to the oscillator inverter on the Sine-source Assembly (page 7.6-1), and thence to the −15V rail.

With constant input current, the mirrors continue to draw the same output current from the AN4 bias network for Q29, so the frequency of the dual-integrator oscillator remains constant. Thus the loop stabilizes only when the oscillator frequency is in phase with (and therefore at the same frequency as) the Frequency Synthesizer output.

The overall action is for a lagging oscillator (frequency lower than the synthesizer) to increase the DC current flowing into the two current mirrors, and vice-versa if the oscillator leads. The two inputs to the comparator are in phase when the sinewave output from the oscillator is at the synthesizer frequency.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M30. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

4.8.8 Oscillation Amplitude Detector

The method of amplitude measurement relies on the identity '$\sin^2\omega t + \cos^2\omega t = 1$' to convert AC output signals from the oscillator into a representative DC signal.

Squaring $A\sin\omega t$ and $A\cos\omega t$:

$$A^2\sin^2\omega t = \frac{A^2}{2} - \frac{A^2}{2}\cos 2\omega t$$

$$A^2\cos^2\omega t = \frac{A^2}{2} + \frac{A^2}{2}\cos 2\omega t$$

The AC waveforms of $A^2\cos^2\omega t$ and $A^2\sin^2\omega t$ are inverted versions of each other, at twice the original frequency, and both are symmetrical about the DC mean value of $\frac{A^2}{2}$.

By summing the two, the AC waveforms are eliminated, leaving a DC signal, A^2, representing the square of the amplitude.

In the Amplitude Detector, the Vsin and Vcos outputs from the oscillator are squared electronically and summed as a differential current I^2. This is compared with a constant DC reference current I_{ref} to generate the error current ($I^2 - I_{ref}$), which is passed through resistors to derive an amplitude error voltage 'V_G'. This is filtered and passed to the Amplitude Control circuits (page 7.6-5).

V_G is driven to zero by the action of the amplitude control loop, so that $I^2 - I_{ref} = 0$, and thus $I^2 = I_{ref}$. The loop will therefore stabilize only when the two are equal, at a constant amplitude.

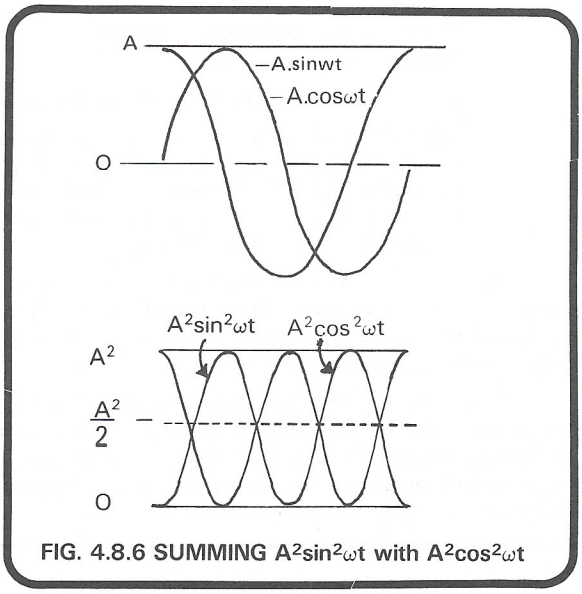


FIG. 4.8.6 SUMMING $A^2\sin^2\omega t$ with $A^2\cos^2\omega t$

4.8.8.1 Squaring Circuit Inputs
(Circuit Diagram 430446 Page 7.6-1)

Vcos and Vsin are squared independently in a pair of differential 4-Quadrant multipliers, each with two identical differential inputs. The Sine Squarer receives $V\sin\omega t$ from the second integrator M30 (Q44 emitter), and $-V\sin\omega t$ from the main inverter (M15-6). As $+V\cos\omega t$ is the only natural cosine output from the oscillator, $-V\cos\omega t$ is derived by inversion in M31. These are both fed as inputs to the Cosine Squarer.

4.8.8.2 Cosine Squarer
(Circuit Diagram 430446 Page 7.6-2)

Isolating the Cosine circuit alone as an example, there are two differential inputs. One is applied across M34 pins 13 and 16, and the other across pins 6 and 10.

The multiplying action of the squaring circuitry relies on the exponential transconductance between a transistor's base voltage and its emitter-collector current:

$$I_c \propto \exp(V_{be})$$
$$\text{and } V_{be} \propto \text{Ln}(I_c)$$

The difference between the currents in M34-1 and M34-14 collectors is linearly proportional to $V\cos\omega t$ (due to M34 emitter resistors AN15). The currents are drawn from the supply through Q55 (which is connected as two matched diodes), but because of the exponential transconductance, Q55 base-emitter voltages increase logarithmically with increase of emitter current. Therefore the differential voltage at Q56 and Q57 bases due to Q55 emitter currents is logarithmic:

$$V_{Q55\text{-}4} - V_{Q55\text{-}3} \propto \text{Ln}(V.\cos\omega t)$$

The difference between the currents in M34-9 and M34-7 collectors is also linearly proportional to $V\cos\omega t$ (due to other M34 emitter resistors AN15). But each collector current is divided between the two halves of the dual transistor in its collector circuit, regulated both by the dual transistor's exponential transconductance, and by its logarithmic differential base voltage.

The combined effect of these two factors is similar to the mathematical operation of multiplying by adding logarithms: a term is produced in each Q56 and Q57 collector current, proportional to the linear product of the two input voltages.

By cross coupling the collectors of Q56 and Q57 as shown, other constant terms are suppressed, and the difference between the currents drawn from AN15-7/8 and AN16-9/10 is proportional to:

$$V\cos\omega t \times V\cos\omega t$$

The inputs are equal, so the differential output current is proportional to $V^2\cos^2\omega t$.

4.8.8.3 Sine Squarer

The Sine Squarer behaves in the same way, producing a differential current in its collector loads proportional to $V^2\sin^2\omega t$.

4.8.8.4 Cos^2, Sin^2 and I_{ref} Summing

In the 4200 squaring circuits, the currents from both Sine and Cosine Squarers are combined in common loads. The voltages developed across the loads will therefore also differ by an amount proportional to $V^2\cos^2\omega t + V^2\sin^2\omega t$. Thus if a reference current was not superimposed, and utilizing the well-known identity '$\sin^2 + \cos^2 = 1$', a DC voltage would exist between TP9 and TP10 (TP9 positive), equal to:

$$KV^2(\cos^2\omega t + \sin^2\omega t) = KV^2$$

where 'K' is a constant at constant temperature, dependent upon identical circuit values in both squarers, and 'V' is the amplitude of both sine and cosine outputs from the oscillator.

However, a reference current is superimposed. The DC current I_{ref} is drawn through the 1kohm load AN15 by M40 (pin 2), reducing the positive value of TP9 voltage with respect to TP10 to $(KV^2 - KV_{ref})$. The reference current is established at a value which includes the scaling factor 'K', by D26 and R91. (The value of R91 for correct oscillator amplitude is determined at manufacture). M34 is connected as a diode to compensate for M40 V_{be} temperature drift.

Voltage $K(V^2 - V_{ref})$ is applied to the input of M35a, the unity-gain Summing Amplifier. M35a is connected to remove any common mode present at its input, so at TP11, $K(V^2 - V_{ref})$ is referred to common 2A. At this point it can be recognized as the Amplitude Error Voltage. Moreover, the amplitude loop adjusts the oscillator outputs to drive the error voltage to zero, so the action of the loop also drives V^2 to equal V_{ref}.

4.8.8.5 Filtering

Because components cannot be matched exactly, some small differences can exist between the $\sin^2$ and $\cos^2$ terms. Such differences appear in V_G as the fundamental and second harmonics of the oscillator frequency. These are limited by the filter formed by M35b and its associated circuit.

It would be possible to set a single low-pass bandwidth for all ranges, but as this would need to filter down to 20Hz for the 100Hz range, it would also impose inconveniently long settling times for the higher frequency ranges. The low-pass bandwidth of the filter is therefore switched between frequency ranges by the $R_{4\text{-}\emptyset}$ signals decoded from $FREQR_{2\text{-}\emptyset}$ in the synthesizer (page 7.6-5).

The frequency range signals select the appropriate feedback components, by conduction of only one FET from Q47-Q52 per range.
(Q48 is not used in the 4200).

The filter output is the oscillator amplitude DC error signal 'V_G', limited to a maximum of approx. ± 6V by the action of back-to-back clamp diodes D24 and D25. V_G passes via link B (see page 7.6-1), to the 'Amplitude Control' circuitry. The value of V_G determines the fraction, and its polarity the phase, of the $V.\cos\omega t$ signal which is to be added to $V.\sin\omega t$ at M15 input.

4.8.9 Amplitude Control Implementation
(Circuit Diagram 430446 Page 7.6-1)

Before describing the control circuitry, it is useful to review the various controls imposed on the oscillator (see Figs. 4.8.1 and 4.8.4):

a. Frequency control by phase-locked loop to the frequency of the synthesizer output (albeit with a constant phase lag). This is effected by controlling the gain of the inverter stage of the oscillator. (Input resistance of M15 is changed by adjusting the conduction of FETs Q29.)

b. Phase control to establish exactly 360° loop phase-shift by injecting a small amount of $V\cos\omega t$ into the oscillator inverter input (via R29).

c. Amplitude control by adjusting the sense and amplitude of $V.\cos\omega t$ added to $V.\sin\omega t$, so that the loop gain is exactly unity at 360° loop phase-shift, at a constant output amplitude, and at the synthesizer frequency.
(M23 gain is adjusted by varying the attenuation of its input signal, using Q41a and Q41b.)

Amplitude error is corrected by adding a fraction of $V\cos\omega t$ or $-V\cos\omega t$ to the $V\sin\omega t$ feedback being applied to the main inverter M15. A push-pull control circuit is employed in order to adjust both amplitude and sense. $V\cos\omega t$ is input from Q31 emitter to R71, and its inverse is input to R70 from the output of M31, which also provides the $-V\cos\omega t$ input for the cos squarer.

4.8.9.1 V.cosωt Amplifier — M23

M23 is connected as a summing VCA, with a fixed feedback resistor R53. $V\cos\omega t$ and $-V\cos\omega t$ are applied to opposite ends of its balanced input resistor chain R71, R65, R64 and R70. The center of the chain is the virtual ground of M23, so if the 'on' resistances of $Q41_a$ and $Q41_b$ are equal, the balance is not disturbed and M23 output voltage is zero.

When the Loop-gain Error is zero (V_G = OV), the static conditions set approx. −3V bias on both FETs (depletion mode) to reduce crossover distortion. The FET gates are also bootstrapped by M24 and M25 to half the AC voltage between source and drain.

The DC conditions are:

$Q41_a$	Q46 emitter	—	−0.75V
	M26 I_{in}	—	150μA
	M26 I_{out}	—	300μA
	$Q41_a$ V_{gs}	—	−1.5V
$Q41_b$	M32-6	—	OV
	Q45 emitter	—	−0.75V
	M27 I_{in}	—	150μA
	M27 I_{out}	—	300μA
	$Q41_b$ V_{gs}	—	−1.5V
Amplitude Error:			
	M23-6	—	zero

The Amplitude Error adjusts the 'on' resistance of $Q41_a$ and $Q41_b$ differentially, due to the inverter M32 in the side feeding $Q41_b$. In the case of a positive V_G of about 0.5V:

$Q41_a$	Q46 emit.	—	−0.25V
	M26 I_{in}	—	50μA
	M26 I_{out}	—	100μA
	$Q41_a$ V_{gs}	—	−0.5V (more conduction)
$Q41_b$	M32-6	—	−0.5V
	Q45 emit.	—	−1.25V
	M27 I_{in}	—	250μA
	M27 I_{out}	—	500μA
	$Q41_b$ V_{gs}	—	−2.5V (less conduction)

The output voltage at M23-6 is in the same phase as $V\cos\omega t$, increasing with larger amplitude error.

For a negative V_G, M23-6 output voltage assumes the same phase as $-V\cos\omega t$, increasing with larger amplitude error.

Transistors Q45 and Q46 act as voltage-to-current converters to drive the 'X2' current mirrors M27 and M26. Voltage reference diodes D20 and D22 provide the crossover bias. D21 and D23 provide clamping when Q45 and Q46 bases are driven positive, preventing V_{be} breakdown.

M23 output (now recognized as 'B.cosωt') is summed with the basic oscillator feedback ($V\sin\omega t$) at the main inverter input (M15-5). When the amplitude is correct, and the loop phase is exactly 360°, M23 output is zero and does not inject any 'cos' component into the loop.

If the loop gain or phase is in error, then the squarers' output current is not equal to the reference current, V_G is not zero, and a small amount of cos component is fed into the loop. This adjusts the loop phase and gain to correct the oscillator amplitude.

4.9 OUTPUT AMPLITUDE CONTROL SYSTEM

This complex system generates the whole range of 4200 voltage outputs, as defined by its inputs. For the Current function, an AC voltage is derived from the internal voltage amplitude loop on the 1V or 10V range to act as an accurate reference. Thus the following description applies also to the generation of that reference.

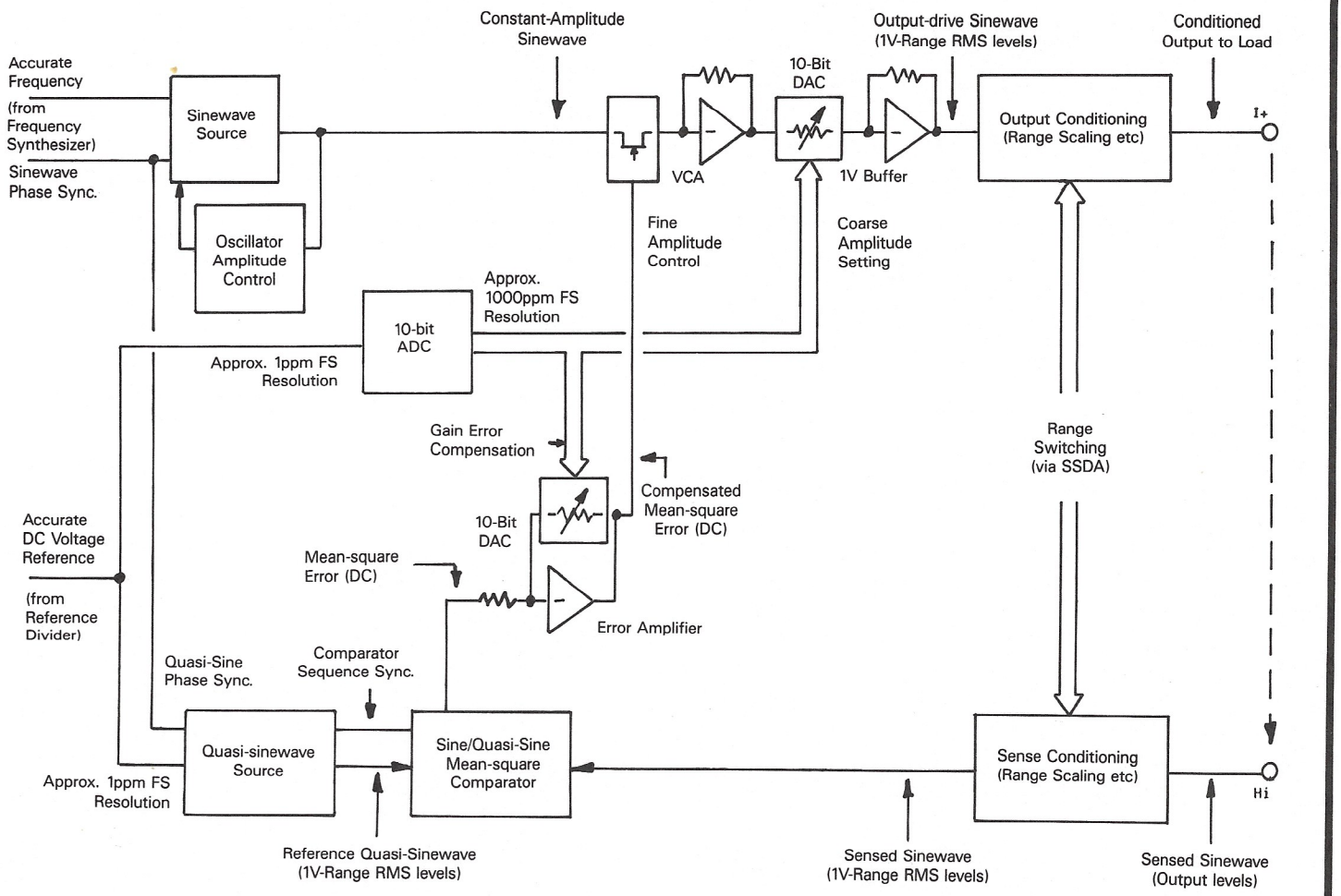


FIG. 4.9.1 OUTPUT AMPLITUDE CONTROL SYSTEM.

Characteristic of 4200 Output	*Controlling Element*	*Controlling Input to Loop*
Frequency:	Frequency Synthesizer (Crystal Sourced)	Constant-amplitude sinewave from Quadrature Oscillator
Sinewave Purity:	Quadrature Oscillator	Constant-amplitude sinewave
Voltage Range:	Processor, via SSDA and Reference Divider Control Latches	Ranging Signals
Coarse Amplitude:	Reference Divider	Accurate DC Reference Voltage (Resolution reduced to approx. 1000ppm of Full Scale by the 10-bit DAC).
Fine Amplitude:	Reference Divider and Quasi-sinewave Generator	Quasi-sinewave RMS value at a resolution of approx. 1ppm of Full Scale.

4.9.1 System Block Diagram (Fig. 4.9.1)

The system elements are described individually in the five sub-sections from 4.10 to 4.14. The system block diagram at Fig. 4.9.1 throws clear of the handbook, so that it can be used for reference when reading these descriptions.

4.9.2 Frequency and Waveshape Control

Sinewave sourcing is the subject of sub-sections 4.7 (Frequency Synthesizer) and 4.8 (Quadrature Oscillator). The result is a high-purity sinewave of constant 1.9V amplitude, input to the VCA.

4.9.3 Output Ranging

The microprocessor passes Voltage and Current range selections into guard via the serial data link as described in sub-section 4.5.

This range information is held in the Analog Control latches in the Reference Divider Assembly, providing signals to the Output and Sense conditioning circuitry. Their effects are described in sub-sections 4.11 to 4.13.

4.9.4 Coarse Amplitude Setting

The 1V Buffer also acts as a coarse amplitude control within each range. The value of its input resistance is adjusted to control its gain, which is incremented in steps of approximately 1000ppm of Full Scale by a 10-bit digital-to-analog converter.

The increments are defined by a 10-bit analog-to-digital converter, which responds to the accurate DC Reference voltages generated by the Reference Divider. The value of the 'DC Ref' voltage is proportional to the values set on the front panel OUTPUT display, as described in sub-section 4.6.

This coarse adjustment of output amplitude allows the fine control element (the VCA) to operate within a small dynamic range, minimizing introduced distortion and thus maintaining the high purity of the output sinewave.

The operation of the coarse amplitude control is described in sub-section 4.10.

4.9.5 Fine Amplitude Control

4.9.5.1 Error Loop

The output amplitude is controlled within the coarse increments by an 'error' loop. The output is sensed at the load for 4-wire connections, or at an internal point in the forward path when 2-wire connection is selected (or imposed).

The sensed output is reduced to 1V Range RMS levels by the Sense Conditioning circuitry (as described in section 4.11 and 4.13), and its mean-square value is compared with that of the Reference Quasi-sinewave. The difference between the two values is expressed as a DC error, and fed to control the gain of the VCA.

Because the coarse amplitude control adjusts the error loop gain, and the error itself results from comparison with an amplitude analog, the gain of the error loop would not be naturally constant. Compensation is therefore applied to the error to reduce the loop gain in synchronism with increasing increments of coarse amplitude. (The Error Amplifier feedback resistance is reduced by a second DAC in step with the coarse amplitude ADC. The result is that the loop gain, and therefore the loop dynamics, are virtually linear.)

Details of VCA operation and error compensation are described in sub-section 4.10.

4.9.5.2 Mean-Square Comparator

When a value is set on the OUTPUT Display, it describes the RMS value of the output. From the displayed value the Reference Divider generates an accurate DC Reference voltage (stepping in increments of approximately 1ppm of Full Scale), which results in a quasi-sinewave whose peak voltage has the same value.

(Thus at 1V Full Range output, the DC Reference voltage and the quasi-sinewave peak voltage are both 1.397V.)

The Crest Factor for any wave is defined as its Peak value divided by its RMS value. For a pure sinewave the figure is $\sqrt{2}$ (say 1.414), whereas the quasi-sinewave crest factor is 1.397. So for the same RMS value of 1V Full Range output, the quasi-sinewave input to the comparator has a peak value of 1.397V, against the feedback peak of 1.414V. The comparison is between mean-square rather than RMS values, but when the mean-square difference is zero, so is the RMS difference.

Generation of DC Reference voltage and Quasi-sinewave are described in sub-section 4.6.

4.9.5.3 Synchronization

The comparator is based on a sequence of squaring, integration, sampling and subtraction. Its operation and accuracy rely heavily on the synchronism of sinewave and quasi-sinewave, each state-change in the sequence occurring at zero-crossings of both waveforms. Thus both waveforms synchronize to clocks from the synthesizer, even when the sinewave is at a multiple of the quasi-sinewave frequency. The comparison sequence cycles once every ten quasi-sinewave periods.

Comparator operation and synchronization details are described in sub-section 4.14.

4.10 VOLTAGE CONTROLLED AMPLIFIERS
(Circuit Diagram 430446, page 7.6-3)

The circuits described in this section perform the following functions:

(1) Modify the output of the Sine Source by coarsely tracking the gain of the output amplitude loop with the requested output voltage, providing stepped coverage of the instrument's dynamic range.

(2) Provide smooth adjustment of gain, within the coarse steps, in response to mean-square error signals from the Sine/Quasi-Sine Comparator.

(3) Impose the settling rate of the true analog DC reference voltage on both the coarse gain adjustment and the mean-square error (AC AMPL ERROR) scaling.

(4) Sense excess currents in the output buffer, providing a $\overline{\text{LIM ST}}$ signal to the CPU via the analog control interface.

All the circuits described in this section are located on the Sine Source Assembly. On the circuit diagram, two voltage-controlled amplifiers are shown:

a. The 1 Volt Buffer, comprising M45, M46 and the discrete output circuit. The buffer's input resistance is controlled by DAC, M43.

b. The main VCA, M48/Q88, whose input resistance is determined by the FET chain Q76 and Q77.

For a general description of the Output Amplitude Control System refer to section 4.9.

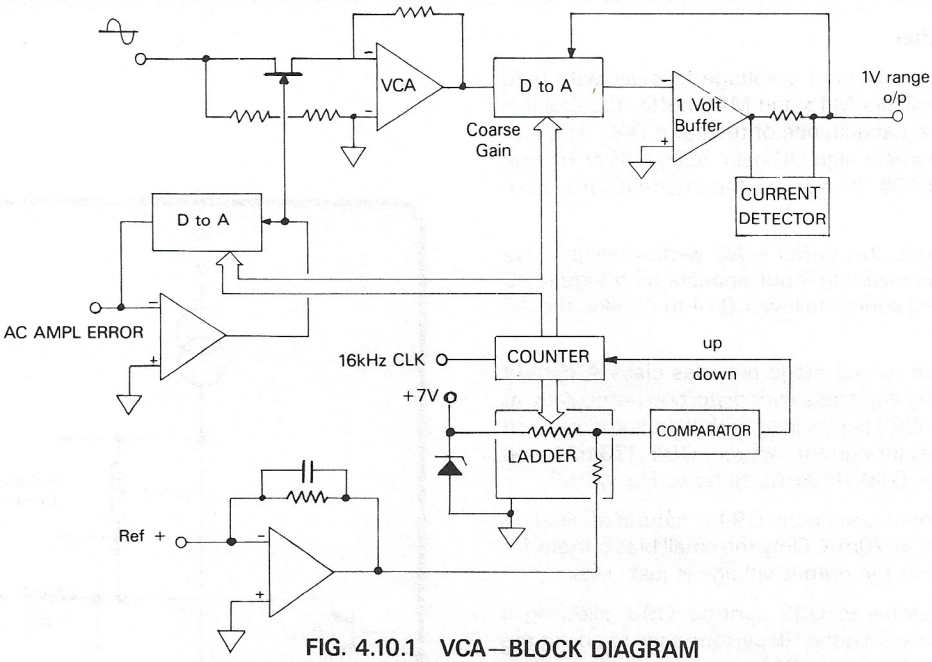


FIG. 4.10.1 VCA—BLOCK DIAGRAM

4.10.1 General (Fig. 4.10.1)

The main VCA receives a constant amplitude sinewave input from the Quadrature Oscillator (Sect. 4.4.8). Its gain is controlled by an error voltage, which is obtained by comparing the sensed sinewave output of the instrument with the reference quasi-sinewave.

The 1 Volt Buffer is included in the output signal path on all voltage and current ranges. It also acts as a VCA, since its input resistance is controlled by its 10-bit Digital-to-Analog Converter. The DAC receives its binary input from an Analog-to-Digital Converter, whose numerical output tracks the user's output demand, in increments of size approximately 1000ppm of full scale.

It is also necessary to ensure that the rate of coarse gain adjustment tracks the settling-time characteristics of the DC Reference filter. To achieve this, the ADC is controlled by the level of the DC Reference voltage. The Reference settling time is thus imposed on the ADC digital output, and hence on the gain adjustments of the 1V Buffer.

For reasons given in section 4.9, it is also necessary to compensate the output loop gain error synchronously with the coarse gain steps. The tracking ADC therefore drives a second DAC, which selects values of feedback resistor in the Error Amplifier. This increments the output-amplitude error loop gain, modifying the AC AMPL ERROR which originated in the mean-square comparator.

The tracking ADC and its DACs ensure that the loop has the fastest possible settling time for any selected frequency.

4.10.1.1 VCA and Buffer

The VCA and 1V Buffer combine in cascade to modify the amplitude of the sinewave output from the sine oscillator, accurately covering the 4200's dynamic range (see Section 4.9). The eventual output from the 1V Buffer (AC 1V FR) forms the instrument's basic 1V range.

The VCA gain is adjusted by the 'AC AMPL ERROR' signal, scaled by M41 and M42. The coarse gain scaling of the 1V buffer derives from the DC Reference voltage 'Ref +'.

4.10.2 Main Voltage-Controlled Amplifier

(Circuit Diagram 430446 Pages 7.6-1 & 7.6-3).

The Sine Oscillator output from divide-by-two buffer M47 (page 7.6-1) is emitter-followed by Q75 to the VCA FET input chain Q76/Q77 (page 7.6-3). These dual FETs are enclosed with M47 PTC feedback resistors R136 and R137, in a metal heatsink. The matched FETS Q76/Q77 ($R_{DS}ON$ within 1%) form the variable gain element for the low input-offset amplifier M48, to provide linear and distortion-free control of gain.

Each FET gate is current-bootstrapped from the divider AN18, to maintain a linear relationship between gain and input voltage. C106 and C117 drive the chain at HF. The centre of the FET chain is also bootstrapped, M44 ensuring precise AC tracking. Resistors R143 and R135 divide and limit the maximum input resistance, preventing the gain from falling to zero.

The thermal linking to M47 feedback resistors compensates for the FET chain temperature coefficient. The inertia of the heatsink's thermal time-constant also prevents gain modulation due to draughts.

The DC signal 'AC AMPL ERROR' is scaled and then fed to each gate by transistors Q78 to Q81, which have low collector capacitance. The voltage control element formed by these transistors adjusts the DC gate voltages of the FETs in the chain, and hence the input resistance of the VCA.

M48 output is emitter-followed and passed through DC-isolating (and AC-compensating) capacitors C121 and C122 into M43, the 1V buffer DAC.

4.10.3 The 1V Buffer

The buffer consists of a voltage follower with hard current limiting. Amplifiers M45 and M46 buffer the Class A power stage from the capacitance of the input DAC. The first buffer M45 has extremely high DC gain, rolling off at HF due to the feedback of C108. It removes the input DC offsets of M46.

M46 controls the buffer's AC performance; C112 ensures that the non-inverting input appears as a virtual AC ground at HF, allowing source-follower Q74 to develop the AC input across R159.

The discrete output stage provides class A current amplification, avoiding any cross-over distortion particularly at HF. Power transistor Q93 is provided with load and quiescent currents, from constant-current source Q94 (70mA) and constant-current sink Q86 (140mA). Refer to Fig. 4.10-2.

With zero input conditions Q94 is saturated, limiting the quiescent current at 70mA. Only the small bias current for Q92 flows in R144, so the output voltage is just +Vb.

The input signal to Q92 controls Q93, allowing a small signal transistor with good HF performance to adjust the large output currents flowing in R144.

Voltage amplifier Q92 cuts off during positive half-cycles of input, reducing Q93 conduction. The quiescent current still flows in R114, but is now shunted through the output circuit via R112 and L7.

During negative half-cycles of input; Q92 conducts, so Q93 conduction increases, drawing its extra (load) current through R144, and its quiescent current from Q94. The emitter of Q92 also attempts to go negative, drawing current directly from the load. The combined currents flow into the current sink, so Q86 must be able to sink 70mA quiescent + 70mA load.

In the output line, inductor L7 and resistor R112 provide phase compensation for capacitive loading at HF.

If any components in the discrete output amplifier are changed, re-adjustment of gain (using M48 feedback resistor R149) may be necessary.

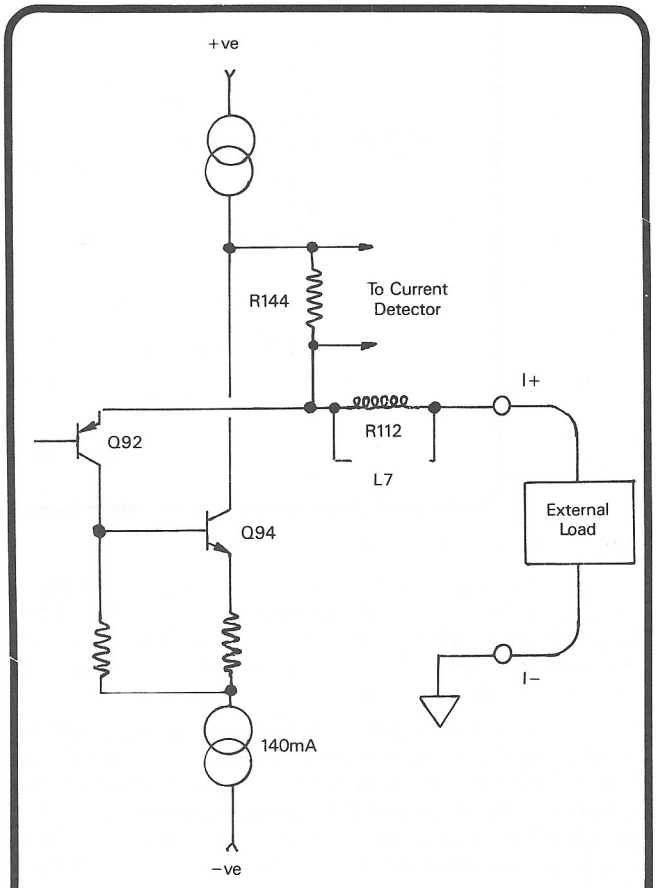


FIG. 4.10.2 1V BUFFER-OUTPUT STAGE

4.10.4 Current Detector

Except for a small bias current, all output current from the discrete buffer stage flows in R144, so the current level can be detected by sensing the differential voltage across it. This sense voltage rides on the output voltage; thus to capture it, the current detector is bootstrapped to the AC 1V output.

High-speed dual comparator M49 forms the basis of the Current Detector circuit. Its supplies are bootstrapped via TP29 to the junction of R144 and R112 in the 1V Buffer output. Q82 and Q84 provide constant current drive to 6.2V Zeners D40 and D41, with Q83 and Q85 providing the regulation for the bootstrapped rails at TP35 and TP36.

The comparator latching levels are set by dividers R151/R152 and R153/R154, their values allowing for bias current error in R144. The comparator's output is open-collector when the peak voltage across R144 is less than the positive or negative latch level. Line drivers Q90 and Q91 are cut off, so the $\overline{\text{LIM ST}}$ line at J6-70 is pulled to +15V by AN2 in the Reference Divider (page 7.4-4).

When the level is exceeded in either polarity, then either M49a or M49b output goes negative. This turns Q90 and Q91 on, pulling the $\overline{\text{LIM ST}}$ line to −15V (in-guard logic-Ø). The signal is passed to the CPU via the serial data link.

This limit is set much lower than the hard current limit of the buffer. If exceeded, the instrument displays 'Error OL', described in Section 2 (Fault Diagnosis). In overload, a built-in margin of safety allows the instrument to meet most of its specifications at 35-40mA.

4.10.5 ADC-DAC Tracking

As mentioned earlier, it is necessary to track the coarse gain stepping rate to the settling-time imposed by the DC Reference filtering. A tracking Analog-to-Digital Converter (ADC) is used to synchronize stepping, ensuring the fastest possible settling time at the selected frequency.

To set circuit conditions for the required output within a range, the gain of the main VCA is set in response to fine amplitude information, in the form of an error signal from the Sine/Quasi-Sine comparator. For constant output amplitude loop gain, the error loop gain also needs to track the coarse amplitude stepping.

For an overall outline of the Output Amplitude Control System, refer to Section 4.9.

4.10.5.1 Use of 'REF+'

(Circuit Diagram 430446 page 7.6-3)

The ADC requires a voltage input which tracks the value of 4200 AC output demanded by the user, with settling times imposed by the Reference filter. The DC 'REF+' voltage exhibits these characteristics, so is used in this circuit to determine the numerical value of the ADC binary output.

'REF+' originates in the Reference Divider and is used to set the peak value of the quasi-sinewave in the AC assembly. Its value ranges from +0.126V at 9% of Full Range, through +1.397V at Full Range, to +2.794V at Full Scale.

REF+ is input to the Sine-Source assembly between J6-57 and J6-56, then applied to amplifier M41b, which is connected to remove any common mode present at its input. Thus at TP47, M41b output is referred to Common-2A.

Capacitors C99, C130 and C131 filter any HF pickup from the reference voltage, and M41b scales up the DC voltage levels by a factor of 2.43, to:

9% of Full Range	: −0.306V,
Full Range	: −3.395V,
Full Scale	: −6.789V.

A positive version of this Full Scale value is also generated (Q66/D30/D31) as a reference for the tracking ADC M38.

4.10.5.2 Tracking ADC M38

(Fig. 4.10.3)

M38 is a 'System DAC' which can be employed either in 'READ' or 'WRITE' mode. WRITE mode is not used in the 4200.

In READ mode the binary count can be output continuously from the ten pins $DB_{9\text{-}0}$. An internal 10-bit counter is clocked at 16kHz into pin 9 via level shifters Q53 and Q54. The counter can be controlled by two level-sensitive inputs: CONT1 and CONT2 (logic-1=+5V; logic-Ø=0V) as follows:

CONT1	CONT2	Effect on Count
Ø	Ø	not used
Ø	1	Incremented
1	Ø	Decremented
1	1	Frozen

An internal 12kOhm reference resistor and switched resistor ladder form a potentiometer between pin 27 (Vref) and pin 1 (Rfb). The junction between them is brought out to pin 2 (OUT1).

The ladder is switched by the 10-bit counter. At zero count it is open-circuit; as the count is increased the ladder resistance reduces in inverse proportion, until at full count of 2^{11}-1 (which corresponds to the 4200 Full Scale output), it reaches its minimum of 12kOhms. See Fig. 4.10.4.

At Full Scale (FS) the M41b output voltage is −6.789V, into Rfb, and the fixed reference into Vref is the positive version of this input, so at FS the OUT1 voltage is balanced at zero.

For 4200 output values below FS, the negative M41b output voltage is linearly reduced, so that the OUT1 voltage tends to increase positively. By feeding an external comparator which drives the CONT1 and CONT2 counter controls, the OUT1 voltage is used to provide automatic control of the count itself. In the case of a reduced output demand, a lower count is required to increase the resistance of the ladder, resetting OUT1 to the zero balance.

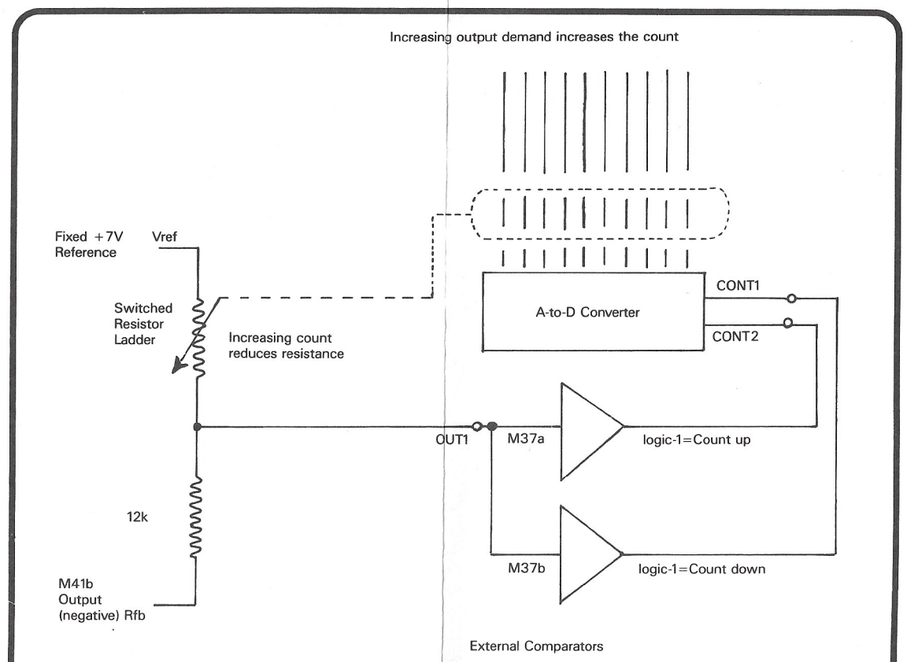


FIG. 4.10.3 SIMPLIFIED DIAGRAM OF TRACKING ANALOG-TO-DIGITAL CONVERTER

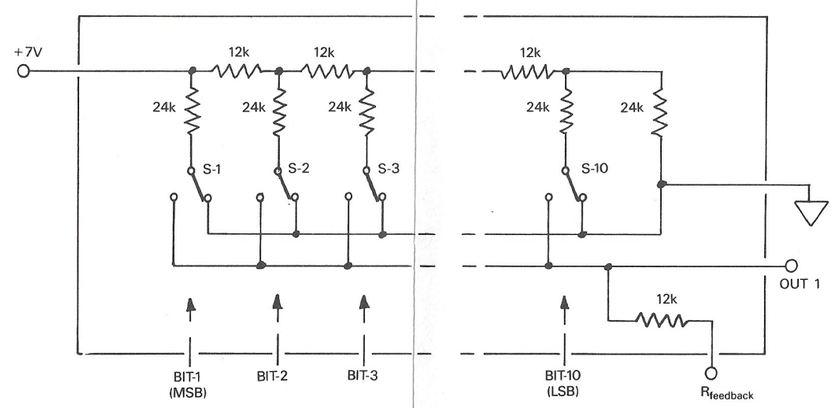


FIG. 4.10.4 A-D TRACKING — R — 2R NETWORK

4.10.5.3 Window Comparator

M37 is a high-speed dual comparator, which accepts OUT1 as its input voltage, and controls the M38 counter via CONT1 and CONT2. The 'Counter Freeze' condition of M38, resulting from both CONT inputs being at logic-1, allows hysteresis bias to be applied the comparator to create the 'Dead Band' window.

Each of the two outputs of M37 responds to its input in the same way: high impedance when its non-inverting input is more positive than its inverting input, and pulled low when the inverting input is more positive (uncommitted-collector).

M37a is connected as a non-inverting device, but M37b inverts its input. OUT1 is input to both circuits. Both inputs are biassed by approximately 15mV to generate the dead-band hysteresis: M37a by R96/R98, R37b by R100/R101.

4.10.5.4 Action for OUT1=Zero

Because of the bias, both M37 outputs are pulled low when the OUT1 voltage is zero. The inverting level-shifters Q67 and Q68 are both cut off by −15V on their gates, so CONT1 and CONT2 are at logic-1. M38 is thus put in the 'Freeze' condition, so its 10-bit output value is held.

In this condition, M36-12 and M36-13 inputs are both at −15V, so M36-10 is also −15V. R99 is therefore placed in parallel with R100, increasing the bias on M37b. The bias on M37a is also increased by Q69 being cut off, placing AN11 and R97 in parallel with R96. The 'Freeze' window is therefore widened, to improve the comparator's noise rejection. Refer to Fig. 4.10.5.

4.10.5.5 Action when OUT1 Voltage Changes

When a user demands a new (greater) output from the 4200, REF+ increases as the Reference filter settles, and the OUT1 voltage becomes more negative. The bias on M37b is eroded and finally exceeded, so M37-7 is placed at high impedance, pulled up to Common-2C by AN13. Q67 conducts, setting CONT1 to logic-Ø and the count increments to step up the gain in the 1V Buffer.

Simultaneously, M36-12 is set to 0V (in guard logic-1). M36-10 rises from −15V to 0V, switching R99 to shunt R101 instead of shunting R100. Q69 conducts, switching R97 to shunt R98 instead of shunting R96. The bias levels shift back to ± 15mV, narrowing the hysteresis window.

If the user had demanded a lower output, OUT1 would have become more positive, exceeding M37a bias. CONT2 would have fallen to logic-Ø, decrementing the counting and reducing the 1V Buffer gain. The effect on the comparator bias would be the same as for the incrementing case.

As the counter changes its numerical value, M38's internal resistance ladder is switched to back-off the OUT1 voltage. When REF+ finally settles, the OUT1 voltage once again enters (and widens) the comparator's dead band, the count freezes, and the 1V Buffer gain remains constant.

Thus the OUT1 voltage remains close to zero as the comparator and tracking ADC respond to the variations of REF+.

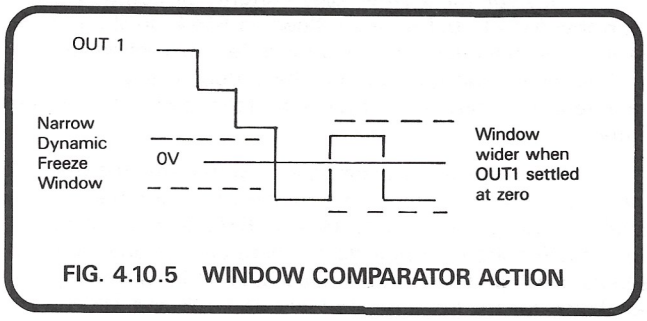
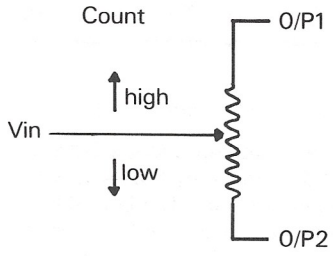


FIG. 4.10.5 WINDOW COMPARATOR ACTION

4.10.5.6 10-bit Digital-to-Analog Converters

M42 and M43 binary inputs are identically connnected, so they both behave in the same way:



For low counts the resistance between Vin and O/P1 is large, and small between Vin and O/P2. The condition is incrementally reversed as the count increases to high values.

As we have seen; an increase in user output demand increases the DC Reference voltage REF+, so a higher ADC count results. This reduces the resistance between M43 pins 15 (Vin) and 1 (O/P1), increasing the gain of the 1V Buffer and thus increasing the 4200 output. This is the coarse gain adjustment referred to in section 9.

M42 has a different function. The fine adjustment of output value is incorporated in the 'Gain Error Loop', in which the output sinewave and quasi-sinewave are compared. The AC AMPL ERROR is generated by this comparison, to be used in controlling the VCA gain.

The error loop thus also passes through the 1V Buffer, and the effect of an increase in ADC count would be to increase the error loop gain, possibly overloading the VCA input FETs. This is prevented by reducing the gain of the error amplifier M41a, using M42 to track the steps of the coarse gain adjustment.

With an increase of the ADC count, M41a feedback is increased, as the resistance between M42 pins 15 and 1 is reduced. This reduces the error loop gain to compensate for the increase due to M43. Thus the fine gain remains virtually constant over the full span of coarse gain adjustment.